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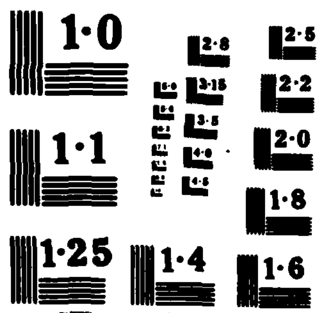

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CONTROL AND SIGNAL CONDITIONING
CIRCUITS FOR E.I.R.M.A.

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This report describes the control and the signal conditioning circuits for the Energetic Ion Retarding Mass Analyzer (EIRMA). The control electronics executed commands received from a main control unit of a multi-instrument rocket experiment. The received instructions were converted into the control signals for the ion mass filter. Signal conditioning was provided.

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I. INTRODUCTION

The Energetic Ion Retarding Mass Analyzer (EIRMA) was developed by the Ionospheric Disturbances and Modifications Branch of the Ionospheric Physics Division of the Air Force Geophysics Laboratory for use in the Beam Emission Rocket Test-1 (BERT-1). During the experiment, the potential of a section of a sounding rocket payload was to be modified with respect to the ambient plasma. The vehicle was to be charged positive by the ejection of electrons and negative by the positive ion ejection. Also, the operation of an automatic spacecraft discharge system was to be tested. During the flight EIRMA was to sample the atmosphere and to differentiate between the ambient ions and the energetic ions emitted and created during the vehicle charging and discharging experiments. It also was intended to survey the energy distribution of selected ions.

The instrument was a quadrupole positive ion filter capable of performing a mass scan analysis between 4 and 100 atomic mass units. A mode to detect all positive ions above the atomic mass unit of 80 was also available. To differentiate between the ions at the various energy levels, a program controlled ion retarding potential was available in the instrument.

The capabilities and the physical structure of the instrument were defined by the Ionospheric Disturbances and Modifications Branch. The Branch was also responsible for the design, construction and the packaging of the quadrupole mass filter including the electronics for the excitation signals. The control electronics which accepted and executed the commands from the main controller of the BERT-1 experiment were designed and constructed by the Electronics Research Laboratory of North-

eastern University. The electronics included the communications interface circuits. Circuits to convert the received instructions into the command signals to control the operation of the mass filter and to generate and set the retarding potential also were the responsibility of the Electronics Research Laboratory. Data conditioning and function monitor circuits were also included in the control electronics package.

The first part of this report describes the operation and the interaction between the various circuits during the execution of the commands. The control of the mass filter and the ion retarding potential, as well as the data conditioning processes are also described in this portion of the report. The second part deals with individual circuits and the description of their functions.

II. OPERATION OVERVIEW

The control circuits for EIRMA were designed to accept digital commands and operating parameters from the master controller of BERT and to convert them into the analog signals to control the operation of the mass filter. Analog control signals were provided to the circuits generating the excitation for the quadrupole and to the high voltage supplies producing the necessary ion retardation potential. The data processing circuits, floating on the retarding potential, amplified the slowly varying ion flux and the mass spectrum signals and converted them into a frequency modulated pulse trains for transmission through optocouplers to the signal conditioning circuits operating at the vehicle potential. There the data was recovered and conditioned for transmission, together with the monitor data, through the telemetry system of BERT. A simplified block diagram of Eirma is shown in Figure 1.

A. Command Interface

The commands and the control parameters for EIRMA were stored in the memory of the master controller of BERT. A 16 line parallel bus was used to transfer the required information from the master controller to the control circuits of EIRMA. It was expected that the instruments of BERT ejecting electrons or positive ions from the vehicle would generate large amounts of electromagnetic interference. To minimize the possibility of errors in the control data, due to that interference, the bus was isolated from all of the instruments by optocouplers.

Twelve lines of the bus were used to communicate the commands and the operating parameters to EIRMA. The remaining four were reserved for the transfer control functions. The four MSB's of each 12 bit control word identified the nature and the destination of the data contained in the 8 LSB's. Thus, the data, which defined a single parameter of a task to be performed by EIRMA during the next mode of operation, was stored in an appropriate temporary memory location of EIRMA identified by the 4 MSB's of the control word. When the control word was identified by its MSB's as a command, the LSB's were disregarded. The 16 possible identification codes and the corresponding commands or task parameters are described in the Appendix A.

When EIRMA was ready to accept a new control word, a bus line designated to identify that state (RDY), was set high. After the master controller, at its convenience, placed the new data into the bus, it pulled another one of the transfer control lines low ($\overline{STR}$). The negative transition on the $\overline{STR}$ line was interpreted by EIRMA as a signal that the control word on the bus was stable and ready to be accepted. After the data or the command on the bus was accepted, the RDY line was

pulled low to signal that EIRMA has indeed accepted the data. When EIRMA was ready to accept the next control word, the line was returned to its high state. The data transfer, one control word at a time, could take place while the instrument was executing the tasks commanded during the previous data transfer. Once all of the data for the next mode of operation has been transmitted to EIRMA, an END OF DATA (EOD) command code could be issued by the master controller. Upon the reception of the EOD code EIRMA ignored any further attempts to communicate until the program for the mode interval ordered by the previous data transfers was completed once. This condition was signaled to the master controller by keeping the RDY line low. When the execution of the program has been completed once, the RDY line was set high again. The control circuits, if not commanded otherwise, started to repeat the same mode interval program. At this time, EIRMA again became receptive to instructions and commands. Although any one or all previously transmitted instructions could be reissued , if needed, an EXECUTE command was expected at that point during the experiment. The EXECUTE command transferred the instructions from the interim memory locations, where they had been stored since the reception from the master controller, into the operating memory and started their execution. Once the execution of a program commenced, the new data could be fed to the EIRMA control circuits. When the EOD command was by-passed and a set of new instructions were followed by the EXECUTE command, the presently run program was aborted and the new instructions were executed immediately. Thus, the EXECUTE command provided the synchronization between the events of BERT and the measurements of the mass filter. The EOD command protected, to a large extent, the new instructions and the program

being run, for at least one complete cycle, from the noisy environment created by the experiment.

In the event that the EIRMA controller "crashed" an internal hard-wired circuit reset the controller and executed a default mode program. This condition was signaled to the master controller by pulling yet another designated transfer control line low. A new set of instructions, followed by the EXECUTE command, once again set EIRMA into the desired operation. The fourth of the transfer control lines was used to reset the controller of the EIRMA and thus to order the execution of the default mode program. The reset could also be ordered by a code transmitted over the bus as a command word.

B. Exciter Control

Four parameters were required to define an analog signal for the control of the quadrupole exciter during a mass scan. Two instructions defined the beginning and the end levels of a staircase signal generated by an 8 bit digital to analog (D/A) converter. The other two instructions were needed to define the height of the steps in the staircase signal and the time duration spent at each step. All steps within a scan were of the same size. They could be selected to range from one to 255 least significant levels in height. The time spent at each step could be programmed to extend from 0.5 to 127 milliseconds in 0.5 millisecond increments. Regardless of the size of the step increment, a scan always ended on the specified end level or on the full scale output voltage of the D/A converter set at +10 volts. A zero step height or dwell time specification produced a dc output at the specified scan start level. This analog signal controlling the mass scan was accepted by the quadrupole exciter circuits at the vehicle potential.

An additional control parameter associated with the operation of the mass filter defined the ratio between the dc and the ac components of the quadrupole excitation. This parameter controlled the duty cycle of a pulse width modulated waveform. This waveform was transmitted through an optocoupler to the output circuits of the exciter operating at the ion retarding potential. There, the necessary dc component was generated by tapping a portion of the ac component from the output windings of the excitation transformer, passing it through a rectifier and gating the resulting signal into a voltage divider-filter. The pulse width modulated signal from the EIRMA controller was used to generate the gating waveform. The duty cycle of the 8 kHz ratio control signal could be defined with a 6 bit resolution between 21.5% and 78.5% of the period. Codes defining the duty cycle outside of these limits produced a dc ON or a dc OFF at the output of the optocoupler.

C. Retarding Bias Control

Two sources could be selected to provide data for the control of the ion retarding bias. One of the sources was a voltmeter measuring the potential of an electrically isolated segment of the vehicle with respect to the main body of the vehicle containing the mass analyzer and other instruments. The other source of control was the data in the program stored in the main controller of BERT.

Since the isolated segment of the vehicle was expected to assume the potential of the surrounding plasma, the voltmeter produced an analog signal which tracked and was proportional to the potential difference between the mass filter and the surrounding plasma. That signal was expected to vary between + and - 10 volts. When this signal was

selected to control the amplitude of the ion retarding bias, it was sampled at the beginning of each EIRMA mode interval or its repretition. The amplitude of the sample determined the output level of the positive HV supply providing the ion retarding bias. Voltages ranging from -100 to +4500 volts could be generated with an approximate resolution of 24 volts. Only the negative signal representing a negative vehicle/plasma potential from the isolated segment voltmeter was thus converted. A sample of a positive signal, regardless of its amplitude, produced a fixed -100V bias.

There were three modes in which the data from the main controller could be utilized to establish the retarding bias. In one of the modes the -100V fixed bias was provided. The second mode selected a fixed positive bias within the limits described in conjunction with the isolated segment voltmeter control. In the third mode, the retarding bias could be scanned between two selected levels in a manner similar to the mass scan control signal. The only difference between the two control signals was in their resolution. While the mass scan had an 8 bit resolution, the retarding potential scan operated with a 7 bit resolution. Since the mass scan and the retarding bias scan were mutually exclusive events, the same codes describing the four control parameters were used for both. A code was assigned to inform EIRMA controller of the role reversal.

A safety feature was included in the control circuits to protect the circuits operating at the high potentials from damage during testing, adjustment and/or calibration. It was a simple measure intended to protect the circuits from a possible damage due to a voltage breakdown at unacceptable gas pressures by preventing an accidental full turn-on of the instrument. When a safety connector was in place,

the maximum amplitude of the retarding potential was limited to below 300 volts. Also, the power to the Channeltron bias and the electrometer supplies was interrupted. A signal was provided to the exciter circuits which was used to limit the amplitude of the ac component of the quadrupole excitation to an acceptable level.

D. Data Conditioning

Nine analog data and monitor signals in the range of 0 to +5 volts were provided for transmission through the telemetry system of BERT. Four of the signals carried the principle data, while the other five provided diagnostic monitoring. The ion mass spectrum, the ion flux, mass identification and the ion retarding bias signals were the primary data. The monitors included the Channeltron bias voltage, the quadrupole exciter primary signal amplitude, the temperatures of the exciter and the dc-to-dc converter circuits and the output of a pressure transducer.

Logarithmic current amplifiers were used to convert the ion flux and the ion mass spectrum currents into the voltage signals. The converters were designed to produce a one volt change in the output for each decade of the input current. The expected range of the positive ion flux current was between 10^{-13} and 10^{-7}A, while the ion mass spectral current from the Channeltron was in the -10^{-12} to -10^{-6}A range. Since the electrometers operated at the ion retarding bias, the data had to be translated to the vehicle potential for transmission through the telemetry; therefore, the slowly varying outputs of the electrometers were converted into frequency modulated pulse trains and transmitted through optocouplers to the recovery circuits. There the process was reversed. The slowly varying signals were recovered and

presented in an acceptable amplitude range to the telemetry system.

To assist in the identification of the species in the ion mass spectrum, the signal from the digital-to-analog converter controlling the mass scan was attenuated and transmitted as one of the principle signals. The retarding bias and the Channeltron bias were monitored directly using high voltage resistors in the input circuits of operational amplifiers. The other monitor signals were conditioned for telemetry using various operational amplifier configurations as required.

Three external power sources were required: $\pm$28 volts and -56 volts. An internal dc-to-dc converter generated the required $\pm$ and the +5 volts. The exciter needed the two negative voltage batteries in addition to the positive 28 volts. An average current drain from the 28 volt batteries was 300mA. The current from the -56 volt battery averaged 0.5A with a peak of 1.3A at the maximum amplitude of the quadrupole ac excitation signal.

III. CIRCUITS

The control unit for EIRMA was based on a microcomputer supplemented by CMOS logic. Optocouplers isolated the command bus of BERT from the circuits of EIRMA. Optoisolators were also used where the internal signals had to be transmitted between circuits operating at vastly different reference bias. To convert the digital commands and data into the analog signals required to control the mass filter and the ion retarding bias, monolythic digital-to-analog interface circuits were employed. When feasable, the analog signals were processed by circuits based on quad operational amplifiers. More specialized monolythic circuits such as very low bias current electrometer operational amplifiers and voltage to frequency converters were employed when needed. The circuits were constructed by wirewrapping component

sockets into perforated fiberglass boards. All power converters were commercially available units. The circuits grouped by their natural interaction and/or placement within the confines of EIRMA housing are shown schematically in Figures 2 through 5.

A. Control Unit

The control unit of EIRMA is shown in Figure 2. The optocouplers U7, U8, U11 and U12 accepted the input signals from the bus. The four bits (A_0 - A_3) carried the commands or the classification codes of the 8 bit data appearing on the lines D_0 through D_7. The resistor networks RN2 and RN3 limited the bus current to the input diodes of the optoisolators. The current was limited to approximately one mA for each diode. U8 also processed the $\overline{\text{STROBE}}$ pulse, instructing the controller that the data on the bus was stable and was intended for EIRMA. The same unit accepted the external RST (reset) pulse. The READY signal, indicating to the main controller of BERT that EIRMA was ready to receive instructions and the $\overline{\text{DFLT}}$ (default) signal, showing that the default program was controlling the operation of the mass filter, were isolated from the bus by OPI 7010 optoisolators.

The data was accepted, interpreted and the appropriate outputs to control the operation of EIRMA were generated by the single chip microcomputer 8751. The operating program, presented together with the flow charts in Appendix B, was stored in the EPROM of the microcomputer. The external interrupt (pin 13) was programmed to respond on the falling edge of the $\overline{\text{STROBE}}$ pulse. Bits 4 through 7 (P2.4 - P2.7) of the I/O port 2 received the data identification code. Data was accepted through the I/O port 1 (P1.0 - P1.7). Once the data was accepted, bit 3 of port 2 (P2.3) was cleared and, through the CMOS OR gate (U6) serving as

a buffer, turned the diode in the optocoupler OPI 7010 ON to acknowledge the reception of the data. Ten μs later the optocoupler was turned OFF and the READY line was returned to its high state.

Two approaches could be used to reset the microcomputer. For a direct reset, the microcomputer could be accessed from a RST line of the bus through the optocoupler U8 and the gate U13. Also, a reset command could be issued on the bus lines A_0 through A_3. A code 9H at the outputs of U7 enabled the AND gates U4. The positive strobe pulse from U8 passed through that gate and the OR gates U13 to the reset pin (9) of the microcomputer. An automatic reset was generated within the control unit whenever the microcomputer failed to execute a prescribed routine. When the chip operated within the program, a pulse issued at P3.2 periodically retriggered the monstable U2. The output at $\overline{Q}$ (pin 7) was in the ZERO state and inhibited the oscillator U3. The output Q (pin 10) of the second monstable in U2 was also reset to ZERO. When the microcomputer failed to trigger the monstable, the output at pin 7 back biased the diode CR1. The oscillator became active. Its output, reshaped into a narrow pulse by the second monostable, propagated through the gates U13 to reset the microcomputer. Once reset, the computer executed the default program to control the operation of EIRMA. The $\overline{\text{DFLT}}$ line on the bus was pulled low to inform the main controller that the default program was controlling the mass filter. The line returned to its high state when new instructions were received from the main controller of BERT and the program for the new mode interval was entered.

The internal digital commands to control the quadrupole exciter and the ion retarding bias were communicated to the digital to analog converters U9 and U10 through the I/O port 0. To boost the

drive capabilities of the port, CMOS buffer U5 and the OR gates U6 were employed. The pull-up resistor network RN1 was used to raise the output levels of the port to the voltages required by the CMOS units. The chip select pulses to latch the data into the appropriate analog to digital converters were generated at P2.0 and P2.1. An 8 bit resolution was used for the control of the exciter, while only the 7 MSB's were used to control the retarding bias. The two MSB's (P0.6 and P0.7) were OR-ed by U6 and presented as the MSB to U10. The ratio control signal, an 8kHz pulse width modulated waveform was produced at P3.1. Pulse widths from 28 to 102μs could be achieved with an approximate 2μs resolution. The MOSFET Q1 was used to drive the diode of an optocoupler which transmitted the waveform to the exciter circuits operating at the ion retarding bias. Bits 4, 5 and 6 of port 3 were used to select the control sources for the ion retarding potential.

B. Retarding Bias Control Circuits

The circuits to control the power supplies providing the retarding bias are shown in Figure 3. When the data in the microcomputer was selected to control the retarding bias, a ONE at pin 1 or U6 (VR1) enabled the AND gate and closed the "switch" between the pins 4 and 9 of the analog data selector U7. Thus, the output of the DAC AD558 was connected to the summing junction of the amplifier formed by U8 and the MOSFET Q_1. R16 served as the feedback resistor of the amplifier. The output of the amplifier provided the power to a high voltage supply (Figure 4) whose output was proportional to the input voltage. A small offset current was injected into the summing junction of the amplifier by R18 and R19 to provide the required minimum input voltage for the supply when the output of the DAC was at zero volts. When the

input of Q_2 (MODE SAFE) was shorted to ground the relay K1 shunted the feedback resistor R16 with R17. The gain of the amplifier was reduced by a factor of 16. Thus, the maximum output voltage of the high voltage supply was limited to approximately 300 volts. Also, the power to the other HV circuits was interrupted (+28V OUT). This safety feature was primarily introduced to prevent voltage breakdown due to an accidental turn-on at reduced pressures. When the relay was in the flight (unsafe) position, +28V were provided to the exciter circuits. There the voltage was used to put the exciter into the full power operation. The dc to dc converter supplying the power to the circuits operating at the retarding bias was also activated. A monitor signal was derived from the +28V by R11 and CR6. This +5V monitor level was passed through an inverter in Figure 2 and continued on as the "SAFEMON" to become a part of a more complex monitor signal in Figure 5.

Since the two MSB's of the microcomputer output were OR-ed into the MSB of the DAC controlling the retarding bias, the output of the DAC reached the full scale value when 7FH were latched into the unit. When the input to the DAC was increased to 80H, the output of the DAC dropped to a half scale value, from where it could be increased back to the full scale value when the digital input reached BFH. The same process repeated itself for inputs between COH and FFH. The MSB of the data was also latched into the pin 13 of U2. When the MSB was a ONE, the outputs of U6 and U5 were driven high. The MOSFET Q_3 turned ON an optoisolator, which in turn switched in a supply floating on the output of the supply controlled by the DAC, (Figure 4). The combined output of the two provided the required retarding bias. Thus, at an input of 7FH two thirds of the full scale output was generated by

the non-floating supply. At 80H again an output of two thirds was generated, but this time by the combined efforts of both supplies. From there, the full scale output could be obtained by increasing the contribution of the ground base supply.

When the isolated sector voltmeter was selected to control the retarding bias, the inverted analog signal at the output of U1 (pin 1) was converted into a digital signal by U3. The conversion was triggered by the selection signal VR2 originating at the microcomputer. The digital word was reconverted into an analog output by U4 which completed the digital sample and hold circuit. As in the previous case, where the microcomputer controlled the retarding bias, the two MSB's of the digital word were OR-ed. The MSB also controlled the status of the transistor Q_3 through the gate U5, provided pin 13 of U6 was high. The status of that pin was determined by the polarity of the isolated segment voltmeter. When the output of the voltmeter was positive, a ZERO was latched into the pin 2 of U2 by the VR2 signal. The AND gate U6 (pin 13) was disabled. A negative signal from the voltmeter enabled that gate. The enabling signal also controlled the status of the switches in U7. When U6 was enabled the switch connecting pins 3 and 9 of U7 was closed. The output of the digital sample and hold circuit was connected to the amplifier U8. The signal generated by the amplifier at the drain of Q_1, using the data derived from the voltmeter, could be modified by the output of the AD558 DAC. The output of the DAC was attenuated by a factor of 5 at pin 8 of U1 before being summed with the voltmeter signal at pin 3 of U8.

If the output of the isolated segment voltmeter was positive when sampled, the transmission gates in U7 between pins 2 and 9 and 14 and

10 were closed. The input voltage to the HV supplies was reduced to zero. Thus, the supplies were forced to shut down. Pin 2 of U2 was reset to ZERO and since VR1 was at ZERO (deselected) the output at pin 10 of U6 was also forced into the ZERO state. This state closed the relay contacts (shown in Figure 4) and applied a negative bias voltage with respect to the vehicle to the front end of the instrument. That bias could also be selected directly by the computer providing a ZERO at pin 9 of U6 (VR3).

C. HV and Data Circuits

The high voltage (HV) bias and the data circuits are shown in Figure 4. The circuits include the ion retarding bias supplies, the Channeltron bias supply and the front end bias relay. Also included are the electrometer amplifiers that were employed to measure the ion flux and the mass spectral data gathered at the retarding bias. They were housed within the same pressurized enclosure as the HV supplies.

Two $\pm$15V dc to dc converters (946) provided the necessary power to the circuits floating on the ion retarding bias. These converters could withstand the large voltage differences between the batteries referenced to the vehicle potential and the floating circuits. One of the converters was assigned to provide power to the floating high voltage supplies, while the other powered the data circuits. The power to the floating Channeltron supply K30Z (3000 V max output) was provided through an operational amplifier arrangement of U1 and the MOSFET Q_1. The output of the supply was fed back through R8 to the summing junction of the combination. The Channeltron bias level was set by the potentiometer R3.

The floating K15Z supply boosted the amplitude of the ion retarding bias (VR). It was provided with the maximum allowed input voltage

of 15 volts through the switch Q_2 and produced 1500V output when activated. The switch was controlled through the optoisolator (OPTO 3) by the control circuits previously described. The K30Z supply referenced to the vehicle potential (ground) provided the controlled portion of the retarding voltage. When a fixed negative retarding bias was needed, the power to the HV supplies K30Z and K15Z was interrupted. The -100 volt unit PS8100 floating on the -56 volt battery provided the necessary bias through R11. The diodes CR2, CR2A and CR3 prevented an excessive attenuation of the negative retarding bias by isolating it from the various resistances to ground. CR2 served yet another purpose. The output of the controlled K30Z retarding bias supply could be reduced only to a minimum of approximately +200 volts before it reached a point of marginal operation. Therefore, to achieve a controlled retarding bias below that minimum, the CR2 diode was chosen to be a low leakage 200 volt zener. Thus, by exceeding the zener voltage at the output of the supply, retarding voltages in tens of volts could be generated. The zener, of course, reduced the maximum achievable retarding bias by its voltage drop to 4300 volts.

The front end bias was also obtained from the fixed negative power supply-battery combination. The signal could be attenuated by R_{13} and R_{14}, if needed, before passing through the relay K1. The relay was kept in the active open state and was released to close by the bias control circuit when the mode designated as VR3 was selected (Figure 3).

The magnitudes of the ion retarding bias and the Channeltron bias were monitored. High voltage 100M resistors were used to derive currents proportional to the amplitudes of the voltages. The diodes placed in series with the resistors to prevent excessive loading of the

negative voltage retarding signal also prevented monitoring of that signal. Since the monitored Channeltron voltage was composed of the retarding signal and the negative Channeltron bias, the monitor current was reduced to a very low leakage current of the diode when the magnitude of the positive retarding bias was smaller than the magnitude of the Channeltron bias voltage. To protect the circuits that processed the monitor currents, both monitor resistors were terminated by diodes connected to the vehicle potential.

The electrometer amplifiers U2 and U4 were configured into logarithmic current to voltage converters. The amplifier U2 accepted the negative current from the Channeltron representing the ion mass spectrum, while the U4 unit operated on the positive current produced by the ion flux into the instrument. Both circuits converted 6 decades of input current into a 6 volt output variation. The ion flux meter measured currents in the 10^{-13} to 10^{-7}A range, while the spectrum amplifier accepted currents of -10^{-12} to -10^{-6}A. Both amplifiers had similar configurations and differed primarily in the values and the polarity of components selected to accommodate the directions and the range of the input currents.

Dual high gain transistor Q_5 placed in the feedback path of the electrometer amplifier served as the log element. The transistor with its collector connected to the input accepted the current and performed the classical logarithmic current to voltage conversion. The other transistor within the package reduced the voltage pedestal and thus eleiminated, to a large extent, the influence of the reverse saturation current on the result. The operational amplifier (U3) circuit forced a comparitively large constant current (200μA) to flow in the collector,

and consequently, in the emitter of the second transistor. The resistor divider formed by R_{27}, R_{28} and R_{29} determined the gain of the amplifier. The temperature influence on the signal due to the variation of the junction voltage was minimized by the sensitor R28. To speed the recovery of the circuit from a cut-off state caused by the input current reversals generated by thc transients in tne system, a circuit to inject a current into the input was used. The voltage divider formed by R_{24}, R_{25} and R_{26}, together with the transistor Q_{12} diverted the unwanted current from the input whenever the output of the amplifier (U2) was forced to ge below a preset level.

The output of the logarithmic circuit was inverted and then converted into a frequency modulated pulse train by the circuit of U5. The modulated data signal was passed through the optocoupler (OPTO 1) and reshaped at the vehicle potential by the transistor Q_{10}. The operation of the circuit amplifying the positive ion flux current was very similar to the operation of the mass spectra amplifier just described.

D. Signal Conditioning and Monitor Circuits

The reshaped frequency modulated pulse trains, carrying the data processed by the electrometers, were reconverted into the slowly varying signals by the converter circuits shown in Figure 5. Also shown are the amplifiers processing the monitor currents derived from the retarding potential and the Channeltron circuits. In addition, signal conditioning circuits for the temperature and the pressure transducer data, the exciter signal monitor and the "safe" state indicator were located on the same board and are included in the drawing.

The frequency to voltage converter circuits U5 and U6 used to recover the ion mass spectrum and the ion flux data were identical. To

establish the zero volts reference for the data signals, appropriate offset currents were injected into the summing junctions of U4 (pins 2, 9). The currents were derived from the voltage reference source O_1 through the voltage inverter U3 and the resistors R_{41} and R_{42}. Potentiometers R_{40} and R_{43} provided the adjustment capability. The gain, to establish the 5 volt full scale limit for the data acceptable to the telemetry circuits, could be trimmed with the potentiometers R_{39} and R_{46} located in the feedback loops of the amplifiers. The remaining harmonics generated during the frequency to voltage conversion were removed from the signal by the two pole low pass output filters. To protect the telemetry circuits from possible overvoltages, the outputs of the filters were limited to a maximum of 5.6 volts by the CR11 and CR12 diodes. R_{60} and R_{61} converted the generated data signals from a one volt per decade to 0.9V per decade to accommodate approximately 6 decades of data within the 0 to 5 volt range of the telemetry signal.

The monitor current derived from the retarding potential was converted into a voltage by U1 (pin1). The output, representing 1000 volts of retarding potential per volt, was passed through an inverter and a voltage limiter before proceeding to the telemetry circuits. The small offset introduced by R_4 accounted for the voltage loss in the 200V zener placed in the path of the retarding potential (Figure4). The resistor could be removed when the retarding voltage and not the supply voltage was to be monitored. Also, the output of U1(pin1) was summed with the monitor current derived from the Channeltron bias circuit. This operation removed the contribution of the retarding potential signal to the Channeltron bias monitor current. Therefore, only the Channeltron bias voltage was represented by the signal (V_E) sent through the telemetry.

Two temperature sensors LM235 were included with the confines of EIRMA. One of these was located with the exciter circuits (RF TEMP) while the other (CR4A) monitored the temperature of a dc to dc converter supplying power to the control and the data circuits operating at the vehicle potential. The sensors produced an increment of 10mV for a change of one ^{o}C in the temperature. The offset current through R_9 (R_{15}) established a zero volt output at $25^{o}C$. The maximum temperature was expected to be below $75^{o}C$. It was represented by a full scale output of 5 volts. The dc to dc converter temperature monitor signal was processed in combination with the safe mode indicator. As previously stated, the safe mode limited the operation of the quadrupole exciter and the HV bias circuits to the output levels below the voltage breakdown limits in a partial vacuum. When in the safe mode, the dual JK flip-flop U8 was kept in the reset state by a ONE on the SAFE MODE signal line. The diodes CR6 and CR7 were cut-off. The signal from the temperature sensor CR4A was conditioned by the circuits of U2 and appeared as a dc level at the cathode of the amplitude limiter diode CR5A. When EIRMA was in the flight ready mode, the JK flip-flop U8 connected as a modulo-3 counter, was released from the reset state by a ZERO on the SAFE MODE line. The 8kHz ratio control signal (from Figure2) scaled to approximately one Hz by U7(Q_{13}) triggered the flip-flop. In its sequence, the flip-flop first forward biased CR7 and pushed the output of the amplifier U2 beyond +10 volts. This forced the diode CR6A to limit the output to +5 volts. Next, both diodes CR6 and CR7 were cut-off. In this state the output of the amplifier was determined by the temperature sensor CR4A. In its third state, the flip-flop forward biased CR6 and forced the output of the amplifier into the negative direction. The negative excursion was limited by

CR4 to one diode drop. Thus, the signal to the telemetry system was kept at zero volts. This sequence, repeated once every 3 seconds, could be used to caution the operator that EIRMA was fully operational.

The pressure transducer Syncom model LX1603A was located in the exciter section. It monitored the pressure in the exciter and the HV circuit enclosures which were interconnected. Since the output of the transducer could range between 2.5 and 12.5 volts, its signal was first offset by -215 volts and then attenuated by a factor of 2 in the circuits of U3.

An additional signal originating in the exciter section was processed by the monitor circuits. This signal representing the amplitude of the ac excitation at the primary of the transformer was attenuated and limited by U1 and CR9 before being passed on to the telemetry.

IV. APPENDIX A

EIRMA CONTROL CODES

1. 00H - Address code followed by an 8 bit data code specifies the starting point of an AMU sweep.

2. 01H - Code in conjunction with an 8 bit data code determines the end point of the AMU sweep.

3. 02H - Together with the 8 bit data code specifies the number of levels (0 to 255) by which the AMU sweep control signal is incremented during a sweep. The sweep ends at the point specified by the accompanying data of the 01H code, regardless of the size of the last increment which could cause an overshoot if executed. A ZERO stops the sweep.

4. 03H - And the 8 bit code specifies the time interval spent at each AMU sweep increment. The DWELL TIME = 0.5(FF-NN)H nS. Where 0<NN<FF is the 8 bit data code. A ZERO stops the sweep.

5. 04H - Spare

6. 05H - Code and the three (3) LSB's of the accompanying data select the ion retarding potential control source. The LSB (BIT 0) transfers control to the digital data transmitted in conjunction with the 06H code. The NLSB selects the isolated segment voltmeter output as the control signal. Bit 2 replaces the positive variable high voltage supply with a fixed voltage of -156 volts as the source of the retarding potential.Only one bit at a time may be designated as ONE.

7. 06H - Code and the 8 bit data code determine the output level of the retarding potential source when the digital data stored in the program is selected as the control source by the code 05H.

8. 07H - Spare

9. 08H - Code forces EIRMA controller to interpret the codes 00H through 03H and the accompanying data as the ion retarding potential control codes and the data identified by 06H code as the AMU level definition.

10. 09H - Code in conjunction with the $\overline{\text{STROBE}}$ ($\overline{\text{STR}}$) signal generates a RESET command for the EIRMA controller. The controller switches into the default program.

APPENDIX A (continued)

11. 0AH - Code and the six (6) LSB's of the data code determine the duty cycle of the signal controlling the ratio between the ac and the dc components of the quadrupole excitation signal. Data between 00H and 0CH produce a dc level which turns the ratio control optoisolator input LED ON. Data 33H through 3FH turn the LED OFF. Data 0DH through 32H produce positive (LED ON) pulse widths ranging from 102 to 28μs while maintaining the period of approximately 130μs.

12. 0BH - Reserved for internal use.

13. 0CH - Spare

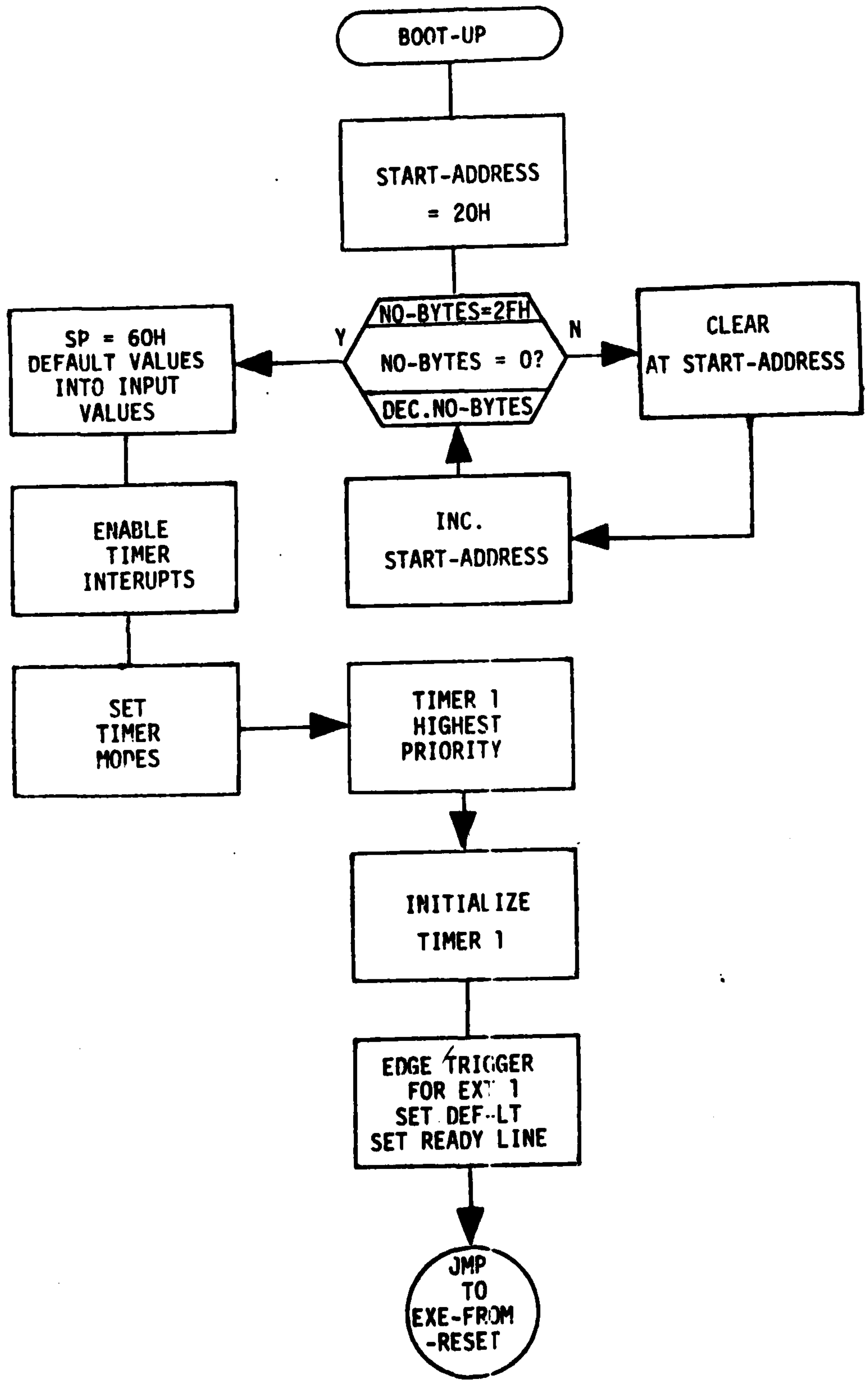
14. 0DH - End of data designator (EOD).

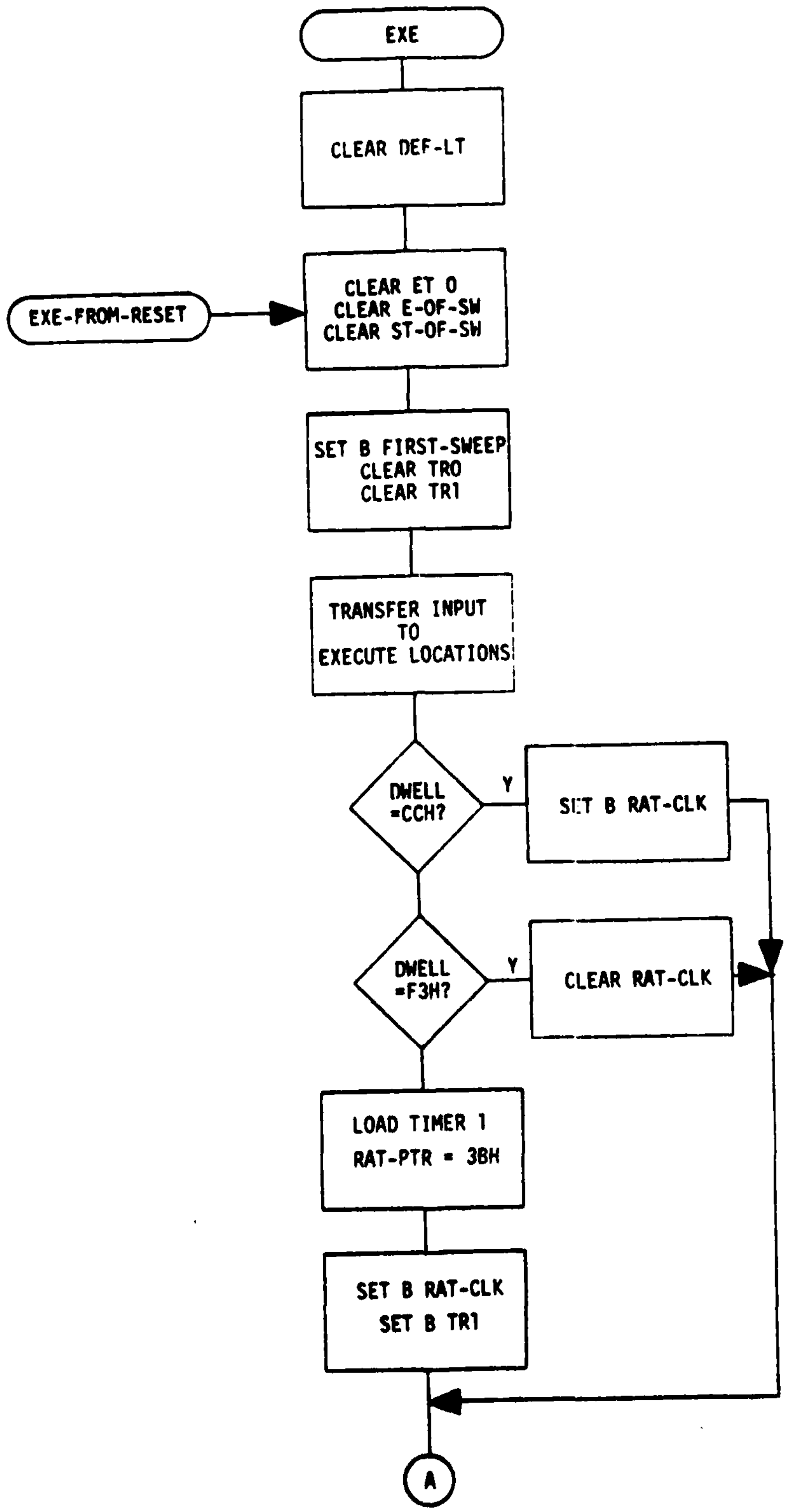
15. 0EH - Starts the execution of the new mode interval program. (EXECUTE)

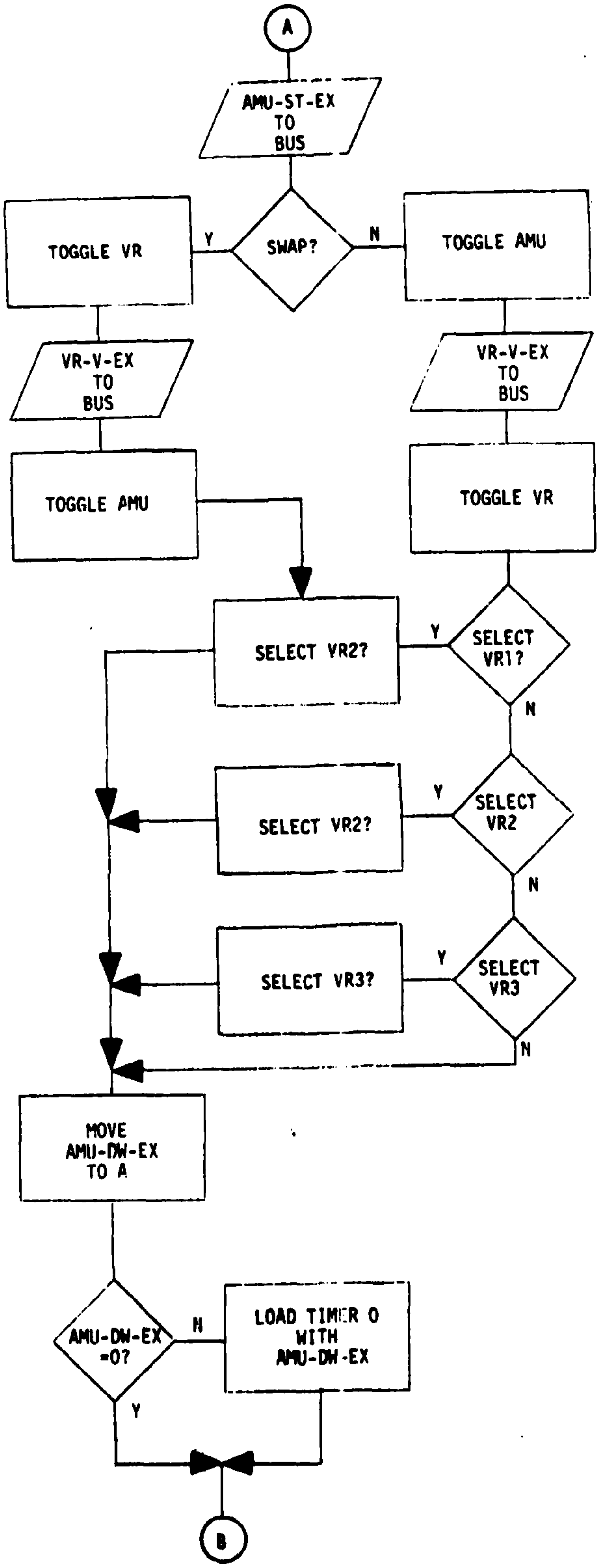
16. 0FH - Reserved for internal use.

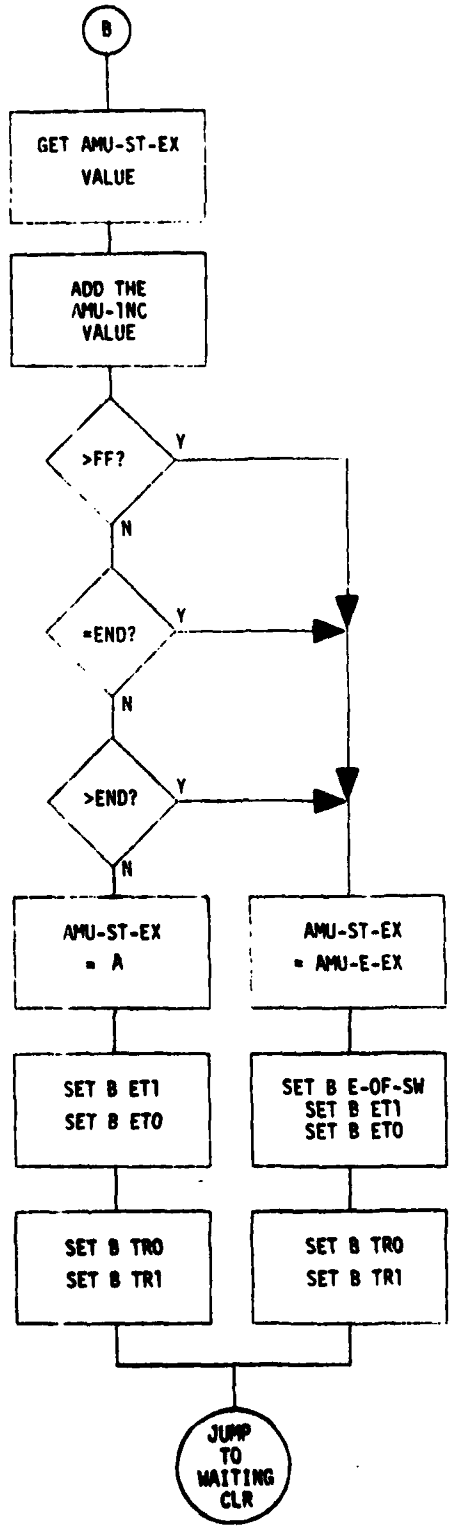
V. APPENDIX B

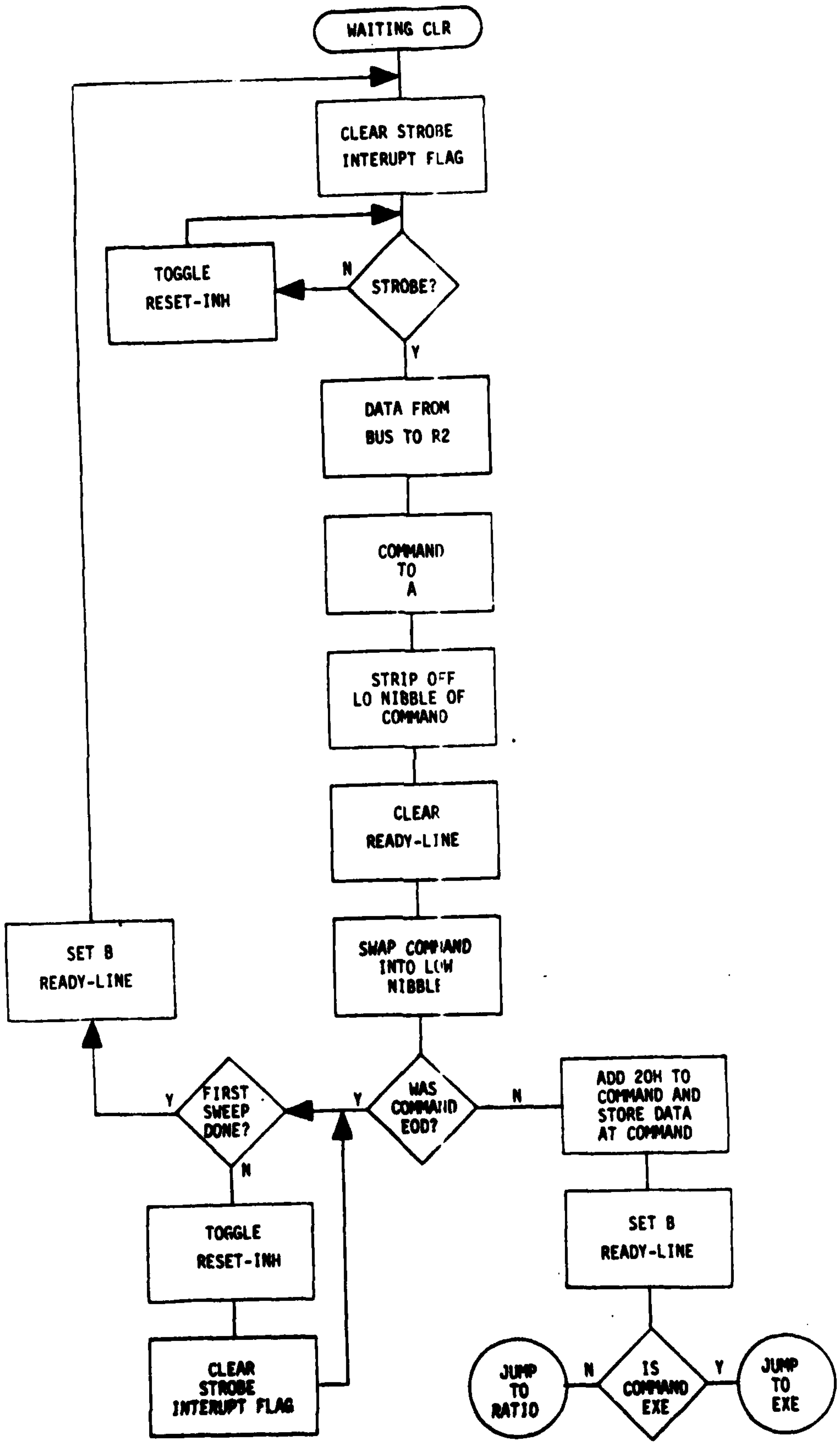
FLOWCHARTS AND PROGRAMS

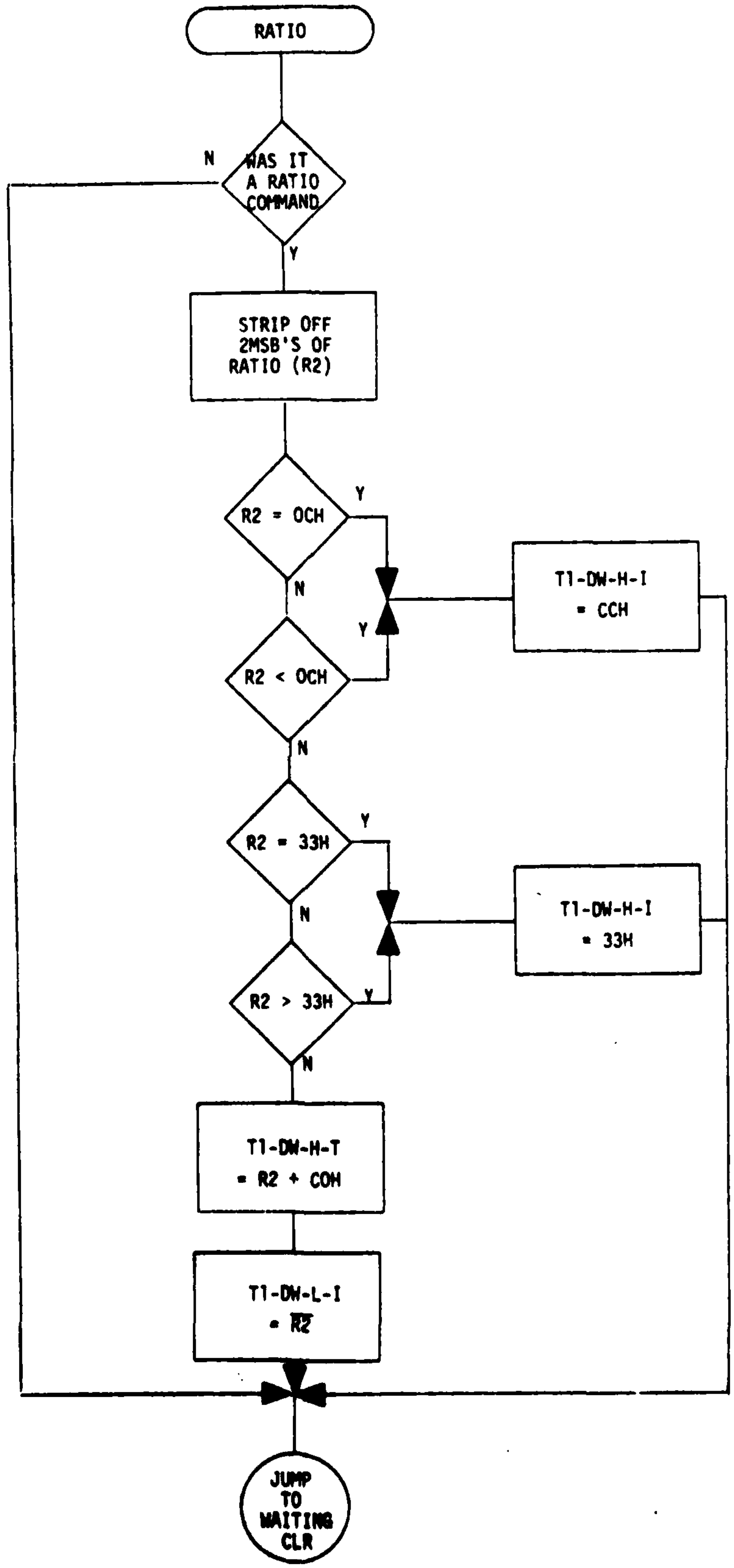


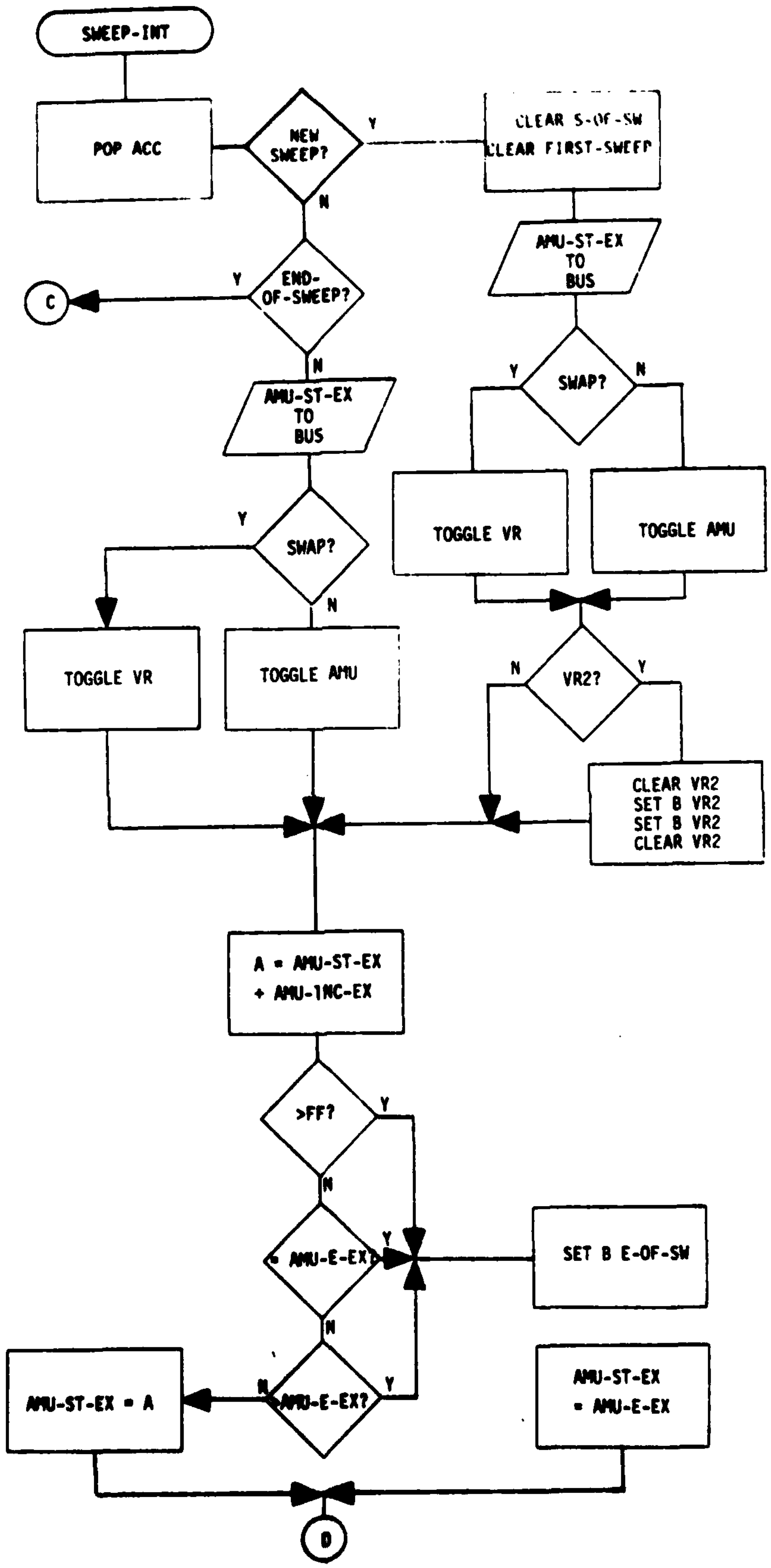

EXE
CLEAR DEF-LT
EXE-FROM-RESET
CLEAR ET 0
CLEAR E-OF-SW
CLEAR ST-OF-SW
SET B FIRST-SWEEP
CLEAR TR0
CLEAR TR1
TRANSFER INPUT
TO
EXECUTE LOCATIONS
DWELL
=CCH?
Y
SET B RAT-CLK
DWELL
=F3H?
Y
CLEAR RAT-CLK
LOAD TIMER 1
RAT-PTR = 3BH
SET B RAT-CLK
SET B TR1
A

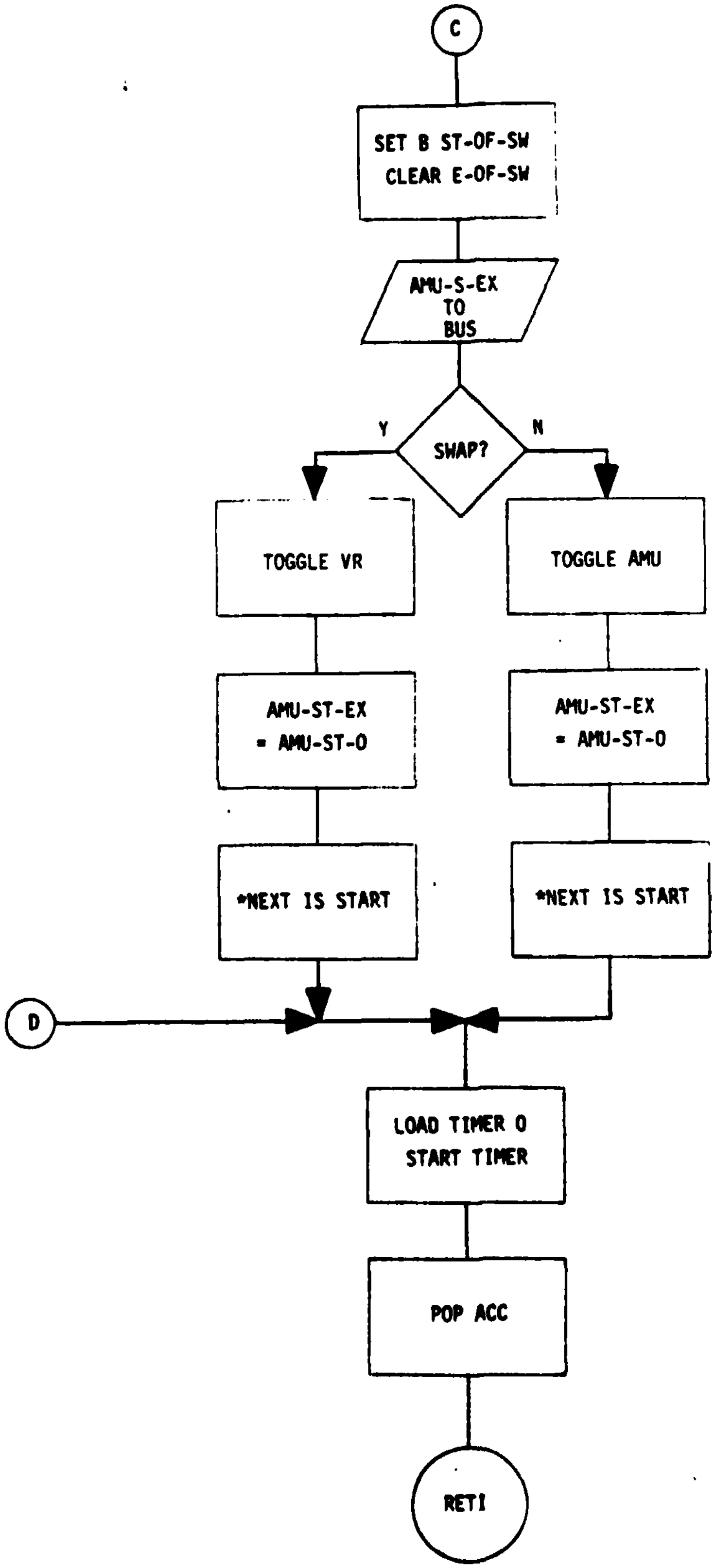

A
AMU-ST-EX TO BUS
SWAP?
Y
N
TOGGLE VR
TOGGLE AMU
VR-V-EX TO BUS
VR-V-EX TO BUS
TOGGLE AMU
TOGGLE VR
SELECT VR2?
Y
SELECT VR1?
N
SELECT VR2?
Y
SELECT VR2
N
SELECT VR3?
Y
SELECT VR3
N
MOVE AMU-DW-EX TO A
AMU-DW-EX =0?
N
LOAD TIMER 0 WITH AMU-DW-EX
Y
B

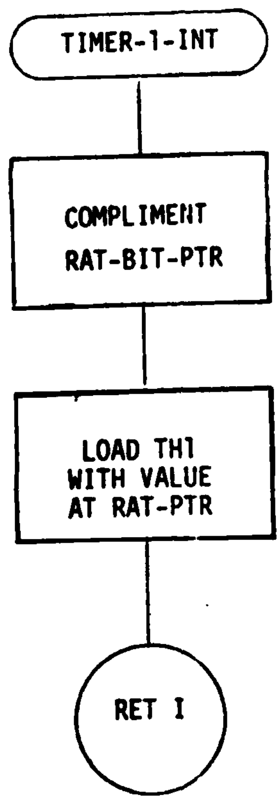

B
GET AMU-ST-EX VALUE
ADD THE AMU-INC VALUE
>FF?
Y
N
=END?
Y
N
>END?
Y
N
AMU-ST-EX = A
AMU-ST-EX = AMU-E-EX
SET B ET1
SET B ETO
SET B E-OF-SW
SET B ET1
SET B ETO
SET B TRO
SET B TR1
SET B TRO
SET B TR1
JUMP TO WAITING CLR


WAITING CLR
CLEAR STROBE INTERUPT FLAG
STROBE?
N
Y
TOGGLE RESET-INH
DATA FROM BUS TO R2
COMMAND TO A
STRIP OFF LO NIBBLE OF COMMAND
CLEAR READY-LINE
SWAP COMMAND INTO LOW NIBBLE
WAS COMMAND EOD?
Y
N
ADD 20H TO COMMAND AND STORE DATA AT COMMAND
SET B READY-LINE
IS COMMAND EXE
N
Y
JUMP TO RATIO
JUMP TO EXE
FIRST SWEEP DONE?
Y
N
SET B READY-LINE
TOGGLE RESET-INH
CLEAR STROBE INTERUPT FLAG


RATIO
WAS IT A RATIO COMMAND
N
Y
STRIP OFF 2MSB'S OF RATIO (R2)
R2 = OCH
Y
N
R2 < OCH
Y
N
T1-DW-H-I = CCH
R2 = 33H
Y
N
R2 > 33H
Y
N
T1-DW-H-I = 33H
T1-DW-H-T = R2 + COH
T1-DW-L-I = $\overline{R2}$
JUMP TO WAITING CLR


SWEEP-INT
POP ACC
NEW SWEEP?
Y
N
CLEAR S-OF-SW
CLEAR FIRST-SWEEP
AMU-ST-EX TO BUS
END-OF-SWEEP?
C
AMU-ST-EX TO BUS
SWAP?
TOGGLE VR
TOGGLE AMU
SWAP?
TOGGLE VR
TOGGLE AMU
VR2?
CLEAR VR2
SET B VR2
SET B VR2
CLEAR VR2
A = AMU-ST-EX
+ AMU-INC-EX
>FF?
= AMU-E-EX?
SET B E-OF-SW
AMU-E-EX?
AMU-ST-EX = A
AMU-ST-EX
= AMU-E-EX
D


C
SET B ST-OF-SW
CLEAR E-OF-SW
AMU-S-EX
TO
BUS
SWAP?
Y
N
TOGGLE VR
TOGGLE AMU
AMU-ST-EX
= AMU-ST-0
AMU-ST-EX
= AMU-ST-0
*NEXT IS START
*NEXT IS START
D
LOAD TIMER 0
START TIMER
POP ACC
RETI


TIMER-1-INT
COMPLIMENT RAT-BIT-PTR
LOAD TH1 WITH VALUE AT RAT-PTR
RET I

```
ISIS-II MCS-51 MACRO ASSEMBLER V2.1
OBJECT MODULE PLACED IN :F1:EIR.OBJ
ASSEMBLER INVOKED BY:  :F1:ASM51 :F1:EIR.SRC

LOC  OBJ            LINE     SOURCE

                             $TITLE(EIRMA AMU/VR CONTROLLER)
                             $DATE(4/11/85)
                             $DEBUG
                             $PAGELENGTH(55)
                             $XREF
                             $NOGEN
                             $EP
                             $INCLUDE(:F1:EIR.DEF)
                     =1      ;
                     =1      ;
                     =1      ;
                     =1      ;****************************************************************************
                     =1      ;*                                                                          *
                     =1      ;*                       EIRMA MEMORY AND DEFINITION SECTION               *
                     =1      ;*                                                                          *
                     =1      ;****************************************************************************
                     =1      ;
                     =1      ;
                     =1      ;  DEFAULT NAMES
 0080                =1      BUS             EQU      P0
 00A0                =1      COMMAND         EQU      P2
 0090                =1      DATA_BUS        EQU      P1
                     =1      ;
                     =1      ;
                     =1      ; DEFAULT VALUES
 0018                =1      AMU_ST_D        EQU      18H
 0070                =1      AMU_E_D         EQU      70H
 0001                =1      AMU_INC_D       EQU      01H
 00F4                =1      AMU_DW_D        EQU      0F4H
 0004                =1      VR_S_D          EQU      04H
 0000                =1      VR_V_D          EQU      00H
 00CF                =1      T1_DW_H_D       EQU      0CFH    ; VALUE = VALUE AS FROM CONTROLLER + C0H
 00F0                =1      T1_DW_L_D       EQU      0F0H    ; VALUE = CPL OF VALUE AS FROM CONTROLLER
                     =1      ;
                     =1      ;
                     =1      ;  MEMORY LOCATIONS
                     =1      ;
                     =1      ;                        E-END
                     =1      ;                        I-INPUT
                     =1      ;                        S-SELEST
                     =1      ;                        ST-START
                     =1      ;                        EX-EXECUTE
                     =1      ;                        O-OPERATIONAL
                     =1      ;                        V-VALUE
                     =1      ;
```

```
LOC  OBJ        LINE     SOURCE

           =1    46     ;
           =1    47     ;
0020       =1    48     AMU_ST_I        DATA    20H
0030       =1    49     AMU_ST_EX       DATA    30H
0034       =1    50     AMU_ST_O        DATA    34H
0021       =1    51     AMU_E_I         DATA    21H
0031       =1    52     AMU_E_EX        DATA    31H
0022       =1    53     AMU_INC_I       DATA    22H
0032       =1    54     AMU_INC_EX      DATA    32H
0023       =1    55     AMU_DW_I        DATA    23H
0033       =1    56     AMU_DW_EX       DATA    33H
           =1    57     ;
           =1    58     ;
0025       =1    59     VR_S_I          DATA    25H
0035       =1    60     VR_S_EX         DATA    35H
0026       =1    61     VR_V_I          DATA    26H
0036       =1    62     VR_V_EX         DATA    36H
           =1    63     ;
           =1    64     ;
002F       =1    65     RAT_PTR         DATA    2FH
           =1    66     ;
           =1    67     ;
002A       =1    68     T1_DW_H_I       DATA    2AH
002B       =1    69     T1_DW_L_I       DATA    2BH
003A       =1    70     T1_DW_H_EX      DATA    3AH
003B       =1    71     T1_DW_L_EX      DATA    3BH
           =1    72     ;
           =1    73     ;
           =1    74     ; BIT LOCATIONS
00B4       =1    75     VR1             BIT     0B4H    ;PORT 3.4
00B5       =1    76     VR2             BIT     0B5H    ;     3.5
00B6       =1    77     VR3             BIT     0B6H    ;     3.6
00B7       =1    78     DEF_LT          BIT     0B7H    ;     3.7
00A0       =1    79     AMU             BIT     0A0H    ;PORT 2.0
00A1       =1    80     VR              BIT     0A1H    ;     2.1
00A3       =1    81     READY_LINE      BIT     0A3H    ;     2.3
0078       =1    82     RAT_BIT_PTR     BIT     78H     ;BIT 0 IN LOC. 2F (T1 DWELL VALS.)
00B1       =1    83     RAT_CLK         BIT     0B1H    ;PORT 3.1
00F0       =1    84     ST_OF_SW        BIT     0F0H    ;START OF SWEEP FLAG
00F1       =1    85     E_OF_SW         BIT     0F1H    ;END OF SWEEP FLAG
00F2       =1    86     FIRST_SWEEP     BIT     0F2H    ;SWEEP HAS JUST STARTED FROM EXE
00B3       =1    87     STROBE          BIT     0B3H    ;STROBE PIN
00B2       =1    88     RESET_INH       BIT     0B2H    ;RESET INHIBIT PIN (PREVENT AUTO RESET)
00F3       =1    89     EXE_INT         BIT     0F3H    ;FLAG THAT THIS WASNT A REAL INT(FROM EXE COM)
           =1    90     ;
           =1    91     ;
                 92     $INCLUDE(:F1:RAMO.MAC)
           =1    93
           =1    94     %*DEFINE(RAM_CLR(START_ADDR,NO_BYTES)) LOCAL SET_TO_ZER
           =1                           (
```

```
LOC  OBJ        LINE     SOURCE

           =1            %'MACRO THAT CLEARS A BLOCK FROM START ADDRESS TO START ADDRES + NO_BYTES
           =1                        %'
           =1                        MOV     R ,%START_ADDR  %'SET R1 TO POINT AT RAM'
           =1                        MOV     R2,%NO_BYTES    %'SET R2 TO CLEAR # OF BYTES'
           =1                        CLR     A               %'GET A 0'
           =1            %SET_TO_ZER:  MOV   @R1,A           %'CLEAR WHERE POINTED'
           =1                        INC     R1              %'POINT AT NEXT LOCATION'
           =1                        DJNZ    R2,%SET_TO_ZER  %'FINISHED ?'
           =1                        %'
           =1                        %'
           =1                        )
                   95    $INCLUDE(:F1:DEF.MAC)
           =1      96    %*DEFINE(DEFPAR)(
           =1            %'****************************************************************%'
           =1            %'*                                                              *%'
           =1            %'*        MACRO FOR DEFAULT PARAMETERS TO BE LOADED INTO EIRMA  *%'
           =1            %'*                                                              *%'
           =1            %'****************************************************************%'
           =1            %'
           =1            %'
           =1                              MOV     AMU_ST_I,#AMU_ST_D
           =1                              MOV     AMU_E_I,#AMU_E_D
           =1                              MOV     AMU_INC_I,#AMU_INC_D
           =1                              MOV     AMU_DW_I,#AMU_DW_D
           =1                              MOV     VR_S_I,#VR_S_D
           =1                              MOV     VR_V_I,#VR_V_D
           =1                              MOV     T1_DW_H_I,#T1_DW_H_D
           =1                              MOV     T1_DW_L_I,#T1_DW_L_D
           =1                              MOV     RAT_PTR,#2AH
           =1            )
                   97    $INCLUDE(:F1:TRANS.MAC)
           =1      98    %*DEFINE(TEMP_TO_EYE)(
           =1            %'***************************************************************%'
           =1            %'                                                               %'
           =1            %'            MACRO TO X-FER INPUT VALUES TO EXECUTE VALUES      %'
           =1            %'                                                               %'
           =1            %'***************************************************************%'
           =1                  MOV     30H,20H
           =1                  MOV     34H,20H
           =1                  MOV     31H,21H
           =1                  MOV     32H,22H
           =1                  MOV     33H,23H
           =1                  MOV     35H,25H
           =1                  MOV     36H,26H
           =1                  MOV     3AH,2AH
           =1                  MOV     3BH,2BH
           =1            )
                   99    $INCLUDE(:F1:TOGGLE.MAC)
           =1     100    %*DEFINE(TOGGLE(BIT_ADDR))
           =1
```

```
LOC  OBJ            LINE     SOURCE

                =1                        %' TOGGLES A BIT/PIN WRITTEN 10/84
                =1           %'
                =1                        CLR     %BIT_ADDR       %'BRING PIN/BIT LOW'
                =1                        SETB    %BIT_ADDR       %'RETURN IT HIGH'
                =1                        %'
                =1                        %'
                =1                        )
                             $INCLUDE(:F1:SELVR1.MAC)
                =1           %*DEFINE(SELECT_VR1)(
                =1           %'*************************************************************************%'
                =1           %'                                  SELECT VR1 MACRO                       %'
                =1           %'*************************************************************************%'
                =1                  CLR     VR2     %'DESELECT VR2 %'
                =1                  SETB    VR3     %'         VR3 %'
                =1                  SETB    VR1     %'SELECT VR1   %'
                =1           )
                             $INCLUDE(:F1:SELVR2.MAC)
                =1           %*DEFINE(SELECT_VR2)(
                =1           %'*******************************************************************%'
                =1           %'                              SELECT VR2 MACRO                     %'
                =1           %'*******************************************************************%'
                =1                  CLR     VR1
                =1                  SETB    VR3
                =1                  CLR     VR2               %'  VR2 IS EDGE TRIGGER  %'
                =1                  SETB    VR2
                =1                  SETB    VR2
                =1                  CLR     VR2
                =1           )
                             $INCLUDE(:F1:SELVR3.MAC)
                =1           %*DEFINE(SELECT_VR3)(
                =1           %'*************************************************************************%'
                =1           %'                                  SELECT VR3 MACRO                       %'
                =1           %'*************************************************************************%'
                =1                  CLR     VR2     %'DESELECT VR2 %'
                =1                  CLR     VR1     %'         VR1 %'
                =1                  SETB    VR1
                =1                  CLR     VR1
                =1                  CLR     VR3     %'SELECT VR3   %'
                =1           )
                             USING 0
----                         CSEG AT RESET
0000 0130                           AJMP    BOOT_UP
000B                         ORG TIMER0
000B 21C1                           AJMP    SWEEP_INT
001B                         ORG TIMER1
001B 21B5                           AJMP    TIMER_1_INT
                             ;
                             ;
                             ;
0030                         ORG 30H
```

```
LOC  OBJ            LINE     SOURCE

                         ;
                         BOOT_UP:        %RAM_CLR(#20H,#1FH)
                                         %DEFPAR
                                         %TEMP_TO_EXE
006F 758160                        MOV   SP,#60H
0072 75A88A                        MOV   IE,#8AH          ;ENABLE TIMER INTERUPTS
0075 758804                        MOV   TCON,#04H        ;SET EDGE TRIGGER FOR EXT 1 INTERUPT
0078 758921                        MOV   TMOD,#21H        ;SET TIMERS T0=MODE 1:16 BIT COUNTER
                         ;                                          T1=MODE 2:8 BIT RELOAD
007B D2BB                          SETB  IP.3             ;SET PRIORITY FOR TIMER1
007D 783A                          MOV   R0,#3AH          ;SET UP R0 RAT_PTR
007F 853B8B                        MOV   TL1,T1_DW_L_EX   ;SET UP TIMER1
0082 853A8D                        MOV   TH1,T1_DW_H_EX
0085 D2B7                          SETB  DEF_LT           ;LIGHT UP DEFAULT LED
0087 D2A3                          SETB  READY_LINE
0089 01C4                          AJMP  EXE_FROM_RESET
                         ;
                         ;
008B 00                            NOP
008C 00                            NOP
008D 00                            NOP
008E C28B                WAITINGCLR: CLR IE1
0090 208B06              WAIT:    JB     IE1,INPUT        ;ON EDGE TRIGGER GO TO INPUT ROUTINE ***JBC
                         WAITING: %TOGGLE(RESET_INH)
0097 80F7                          SJMP  WAIT
0099 AA90                INPUT:   MOV    R2,DATA_BUS      ;GET DATA OFF THE BUS
009B E5A0                          MOV   A,COMMAND        ;       ALONG WITH THE COMMAND ASSOCIATED
009D 54F0                          ANL   A,#0F0H          ;STRIP OFF THE LOW NIBBLE
009F C2A3                          CLR   READY_LINE       ;ACCEPT ALL DATA SO REALY=FALSE
00A1 C4                            SWAP  A
00A2 B40D0F                        CJNE  A,#0DH,NOT_EOD   ;IS IT AN EOD COMMAND?
00A5 30F208              EOD:     JNB    FIRST_SWEEP,EOD_EXIT
                                   %TOGGLE(RESET_INH)     ;PREVENT AUTO-RESET
00AC C28B                          CLR   IE1
00AE 80F5                          SJMP  EOD
00B0 D2A3                EOD_EXIT: SETB  READY_LINE
00B2 80DA                          SJMP  WAITINGCLR
                         ;
                         ;
                         ;
00B4 2420                NOT_EOD: ADD    A,#20H           ;GET THE STORAGE LOCATION FROM THE COMMAND
00B6 F9                            MOV   R1,A
00B7 A702                          MOV   @R1,02H          ;AND USE IT TO STORE R2 (DATA)
00B9 D2A3                          SETB  READY_LINE       ;SHOW THE DATA ACCEPTED
00BB B42E02                        CJNE  A,#2EH,NOT_EXE   ;WAS IT AN EXECUTE COMMAND?
00BE 8002                          SJMP  EXE
00C0 2188                NOT_EXE: AJMP   RATIO            ;IF IT WASNT IT MUST HAVE BEEN RATIO COMM
00C2 C2B7                EXE:     CLR    DEF_LT           ;NO LONGER THE DEFAULT PARAMETERS
00C4 C2A9                EXE_FROM_RESET: CLR    ET0
00C6 C2F1                          CLR   E_OF_SW
```

```
LOC  OBJ         SOURCE

00C8 C2F0                 CLR     ST_OF_SW
00CA D2F1                 SETB    FIRST_SWEEP
00CC C28C                 CLR     TR0
00CE C28E                 CLR     TR1            ;DISABLE TIMERS
00D0 C2A9                 CLR     ET0
00D2 C2AB                 CLR     ET1
                          %TEMP_TO_EXE           ;TRANSFER THE INPUT TO THE EXE LOCATIONS
00EF E53A                 MOV     A,T1_DW_H_EX   ;
00F1 B4CC04               CJNE    A,#0CCH,RAT_NOT_CC      ;IS THE DWELL=0CCH
00F4 D2B1                 SETB    RAT_CLK        ;IF YES
00F6 8014                 SJMP    STRT_TIMER
                  ;
                  ;
00F8 B4F304       RAT_NOT_CC: CJNE        A,#0F3H,RAT_NOT_F3      ;RATIO=F3H?
00FB C2B1                 CLR     RAT_CLK        ;SET UP RAT_CLK PIN TO PROPER LEVEL (=F3)
00FD 800D                 SJMP    STRT_TIMER
                  ;
                  ;
00FF 853B8B       RAT_NOT_F3: MOV TL1,T1_DW_L_EX  ;MOVE EXECUTE VALUE INTO T1 LOW
0102 853A8D               MOV     TH1,T1_DW_H_EX  ;                              HI
0105 752F3B               MOV     RAT_PTR,#3BH   ;SET UP POINTER FOR NEXT INTERUPT
0108 D2B1                 SETB    RAT_CLK        ;SET UP RAT_CLK PIN TO PROPER LEVEL
010A D28E                 SETB    TR1            ;START TIMER1
010C 853080       STRT_TIMER: MOV BUS,AMU_ST_EX  ;PUT START VALUE ONTO BUS
010F E535                 MOV     A,VR_S_EX      ;CHECK IF SWAP IS IN EFFECT
0111 20E310               JB      0E3H,VR_AMU_SWAP;IF SO JUMP
                          %TOGGLE(AMU)
0118 853680               MOV     BUS,VR_V_EX
                          %TOGGLE(VR)
011F 30E015               JNB     0E0H,NOT_VR1
0122 800B                 SJMP    SV1
                  ;
                  ;
                  VR_AMU_SWAP: %TOGGLE(VR)
0123 853680               MOV     BUS,VR_V_EX
                          %TOGGLE(AMU)
                  SV1:    %SELECT_VR1
0135 801E                 SJMP    VR_SELECTED
                  ;
                  ;
0137 30E10E       NOT_VR1: JNB    0E1H,NOT_VR2           ;SELECT VR2?
                          %SELECT_VR2
0146 800D                 SJMP    VR_SELECTED
                  ;
0148 30E20A       NOT_VR2: JNB    0E2H,VR_SELECTED       ;SELECT VR3? IF NO THEN DO NOTHING
                          %SELECT_VR3
                  ;
                  ;
0155 E533         VR_SELECTED: MOV        A,AMU_DW_EX    ;SET UP SWEEP RATE
0157 B40002               CJNE    A,#00H,LOAD_TIMER0     ;00 IS INVALID
```

```
LOC  OBJ            LINE     SOURCE

015A 8008                            SJMP    EXE_INC
                             ;
                             ;
015C 85338C                  LOAD_TIMER0: MOV TH0,AMU_DW_EX          ;LOAD HI BYTE OF TIMER0
015F 758A00                          MOV     TL0,#00                 ;LOW BYTE IS ALWAYS 00
0162 2164                            AJMP    EXE_INC
                             ;
                             ;
0164 E530                    EXE_INC: MOV    A,AMU_ST_EX             ;GET THE NEXT VALUE READY
0166 2532                            ADD     A,AMU_INC_EX
0168 4011                            JC      NXT_IS_LST              ;IF >FF THEN NEXT IS LAST
016A B53102                          CJNE    A,AMU_E_EX,EX_NE_END
016D 800C                            SJMP    NXT_IS_LST
016F 500A                    EX_NE_END: JNC  NXT_IS_LST              ;>END THEN NEXT IS LAST
0171 F530                            MOV     AMU_ST_EX,A             ;SAVE NEXT AS VALID VALUE
0173 D2AB                            SETB    ET1                     ;ENABLE TIMER 1 ** TIMER 1 STARTS IF
                             ;
                             ;
                             ;                                       IF TR1 IS SET **** CO  T   F3 ****
0175 D2A9                            SETB    ET0                     ;ENABLE TIMER 0(SWEEP
0177 D28C                            SETB    TR0                     ;START TIMER 0
0179 018E                            AJMP    WAITINGCLR              ;THEN WAIT
017B D2F1                    NXT_IS_LST: SETB E_OF_SW                ;TELL SWEEP  THAT NEXT IS THE LAST
017D 853130                          MOV     AMU_ST_EX,AMU_E_EX      ;LAST VALUE TO BE OUTPUT
0180 D2AB                            SETB    ET1                     ;START TIMER 1 IF SPST CC
0182 D2A9                            SETB    ET0                     ;START TIMER0
0184 D28C                            SETB    TR0
0186 018E                            AJMP    WAITINGCLR
                             ;
                             ;
                             ;
                             ;
0188 B42A24                  RATIO:  CJNE    A,#2AH,TO_EXIT          ;WAS IT A RATIO COMMAND
018B 53023F                          ANL     02,#3FH                 ;STRIP OFF 2MSB  OF DATA (R2)
018E BA0C02                          CJNE    R2,#0CH,GT_0C           ;DATA=0CH?
0191 8002                            SJMP    SET_RAT_CC              ;IF SO SET IT TO CC (MAX VAL ALLOWED)
                             ;
                             ;
0193 5005                    GT_0C:  JNC     EQ_33                   ;< 0CH JUMP IF GREATER
0195 752ACC                  SET_RAT_CC: MOV T1_DW_H_I,#0CCH         ;0C MINIMUM VALUE ALLOWED
0198 8015                            SJMP    TO_EXIT
                             ;
                             ;
019A BA3302                  EQ_33:  CJNE    R2,#33H,GT_33           ;=33H?
019D 8002                            SJMP    SET_RAT_3F              ;
                             ;
                             ;
019F 4005                    GT_33:  JC      IN_RAT                  ;ACCEPT VALUE IF 33<V<CC
01A1 752A3F                  SET_RAT_3F: MOV T1_DW_H_I,#3FH          ;3F MAXIMUM VALUE ALLOWED
01A4 8009                            SJMP    TO_EXIT
```

```
LOC  OBJ            SOURCE

                    ;
                    ;
01A6 EA             IN_RAT: MOV   A,R2                  ;VALUE IS ACCEPTED BUT NEEDS MASSAGE
01A7 24C0                   ADD   A,#0C0H               ;MAKE WORKING VALUE
                    ;                                      33<V+C0<CC
01A9 F52A                   MOV   T1_DW_H_I,A           ;SAVE IT
01AB EA                     MOV   A,R2                  ;GET ORIGINAL VALUE
01AC F4                     CPL   A                     ;MASSAGE IT
01AD F52B                   MOV   T1_DW_L_I,A           ;SAVE IT
01AF 01BE           TO_EXIT: AJMP WAITINGCLR            ;AND WAIT
                    ;
                    ;
01B1 00             NOP
01B2 00             NOP
01B3 00             NOP
01B4 00             NOP
01B5 B231           TIMER_1_INT: CPL RAT_CLK            ;TIMER JUST INTERUPTS SO SWAP TIMES
01B7 B278                   CPL   RAT_BIT_PTR           ;POINT TO NEXT TIME INTERVAL
01B9 A62F                   MOV   R0,RAT_PTR            ;MOVE POINTER TO R0
01BB 868D                   MOV   TH1,@R0               ; USE IT TO RELOAD TIMER
01BD 32                     RETI
01BE 00             NOP
01BF 00             NOP
01C0 00             NOP
                    ;
                    ;
01C1 C0E0           SWEEP_INT: PUSH ACC
01C3 20F056                 JB    ST_OF_SW,START_SWEEP  ;START A NEW SWEEP?
01C6 20F135                 JB    E_OF_SW,LAST_OUTPUT   ;LAST OUTPUT FOR CURRENT SWEEP?
01C9 853080                 MOV   BUS,AMU_ST_EX         ;GET NEXT VALUE TO BE PUT OUT
01CC E535                   MOV   A,VR_S_EX             ;IS SWAP IN EFFECT?
01CE 20E30F                 JB    0E3H,IS_SWAP
                            %TOGGLE(AMU)
01D5 E530           INC_AMU: MOV  A,AMU_ST_EX           ;GET VALUE JUST PUT OUT
01D7 2532                   ADD   A,AMU_INC_EX          ;ADD THE INC VALUE
01D9 401C                   JC    SET_LAST              ;IF >FF THEN NEXT WILL BE END
01DB B53108                 CJNE  A,AMU_E_EX,NE_LAST    ;= END VALUE?
01DE 8017                   SJMP  SET_LAST
                    IS_SWAP: %TOGGLE(VR)
01E4 80EF                   SJMP  INC_AMU
01E6 500F           NE_LAST: JNC  SET_LAST              ;IF > END VAL THEN NEXT WILL BE LAST
01E8 F530                   MOV   AMU_ST_EX,A
01EA 85338C         SWEEP_EXIT: MOV THO,AMU_DW_EX       ;RESET SWEEP TIME
01ED 758A00                 MOV   TL0,#00H
01F0 D2A9                   SETB  ET0
01F2 D28C                   SETB  TR0
01F4 D0E0                   POP   ACC
01F6 32                     RETI;                                 OUTPUT IS KNOWN (AMU_S_EX)
                    ;
                    ;
```

```
LOC  OBJ            SOURCE

01F7 D2F1           SET_LAST: SETB  E_OF_SW              ;SET END OF SWEEP FLAG
01F9 853130                 MOV     AMU_ST_EX,AMU_E_EX   ;SAVE END VALUE
01FC 80ED                   SJMP    SWEEP_EXIT           ;AND EXIT
                    ;
                    ;
01FE C2F1           LAST_OUTPUT: CLR        E_OF_SW      ;NEXT IS NOT LAST
0200 D2F0                   SETB    ST_OF_SW             ;NEXT IS BEGINING
0202 853180                 MOV     SUS,AMU_E_EX         ;SET LAST VALUE
0205 E535                   MOV     A,VR_S_EX            ;CHECK FOR SWAP
0207 20E70F                 JB      0E7H,LAST_SWAP
                            %TOGGLE(AMU)
020E 853430                 MOV     AMU_ST_EX,AMU_ST_S   ;NEXT IS START
0211 80D7                   SJMP    SWEEP_EXIT           ;AND LEAVE
                    ;
                    ;
                    LAST_SWAP: %TOGGLE(VR)
0217 853430                 MOV     AMU_ST_EX,AMU_ST_S   ;NEXT IS START
021A 80CE                   SJMP    SWEEP_EXIT
                    ;
                    ;
021C C2F0           START_SWEEP: CLR ST_OF_SW            ;RESET FLAG
021E C2F2                   CLR     FIRST_SWEEP          ;HAS COMPLETED AT LEAST SW FROM EX
0220 853080                 MOV     SUS,AMU_ST_EX
0223 E535                   MOV     A,VR_S_EX            ;IS SWAP IN EFFECT?
0225 20E306                 JB      0E3H,START_SWAP
                            %TOGGLE(AMU)
022E 8004                   SJMP    ISO_IN               ;LATCH IN ISO METER ?
                    ;
                    ;
                    START_SWAP: %TOGGLE(VR)
0232 30E1A0         ISO_IN: JNB     0E1H,INC_AMU    ;IF NOT VR2 THEN JUMP
0235 C2B5                   CLR     VR2
0237 D2B5                   SETB    VR2
0239 D2B5                   SETB    VR2
023B C2B5                   CLR     VR2
023D 8096                   SJMP    INC_AMU              ;GET THE NEXT VALUE THEN EXIT
                    END
```

XREF SYMBOL TABLE LISTING
---- ------ ----- -------

NAME	TYPE	VALUE		ATTRIBUTE AND REFERENCES
ACC.	D ADDR	00E0H	A	390 416
AMU_DW_D . . .	NUMB	00F4H	A	29# 136
AMU_DW_EX. . .	D ADDR	0033H	A	56# 312 317 412
AMU_DW_I . . .	D ADDR	0023H	A	55# 136
AMU_E_D. . . .	NUMB	0070H	A	27# 134
AMU_E_EX . . .	D ADDR	0031H	A	52# 325 337 403 4[illegible] 427
AMU_E_I. . . .	D ADDR	0021H	A	51# 134
AMU_INC_D. . .	NUMB	0001H	A	28# 135
AMU_INC_EX . .	D ADDR	0032H	A	54# 323 401
AMU_INC_I. . .	D ADDR	0022H	A	53# 135
AMU_ST_D . . .	NUMB	0019H	A	26# 133
AMU_ST_EX. . .	D ADDR	0030H	A	49# 249 322 328 337 393 [illegible] 411 421 434 442 448
AMU_ST_I . . .	D ADDR	0020H	A	48# 133
AMU_ST_O . . .	D ADDR	0034H	A	50# 434 442
AMU.	B ADDR	00A0H.0	A	79# 253 254 271 272 397 398 431 432 452 453
BOOT_UP. . . .	C ADDR	0030H	A	109 119#
BUS.	D ADDR	0080H	A	20# 249 256 269 393 427 448
COMMAND. . . .	D ADDR	00A0H	A	21# 184
DATA_BUS . . .	D ADDR	0090H	A	22# 183
DEF_LT	B ADDR	00B0H.7	A	78# 168 208
E_OF_SW. . . .	B ADDR	00F0H.1	A	85# 210 336 392 420 425
EOD_EXIT . . .	C ADDR	00B0H	A	189 196#
EOD.	C ADDR	0045H	A	189# 195
EQ_33.	C ADDR	019AH	A	352 357#
ET0.	B ADDR	00A8H.1	A	209 215 333 339 414
ET1.	B ADDR	00A8H.3	A	216 329 338
EX_NE_END. . .	C ADDR	016FH	A	325 327#
EXE_FROM_RESET	C ADDR	00C4H	A	170 209#
EXE_INC. . . .	C ADDR	0164H	A	314 319 322#
EXE_INT. . . .	B ADDR	00F0H.3	A	89#
EXE.	C ADDR	00C2H	A	206 207#
FIRST_SWEEP. .	B ADDR	00F0H.2	A	86# 18 212 447
[illegible]	C ADDR	019FH	A	357 36 #
[illegible]	C ADDR	0197H	A	348 35 #
[illegible]	D ADDR	00A8H	A	160
IE	B ADDR	00B8H.3	A	176 17 194
IN_RST	C ADDR	01A6H	A	361 36 #
INC_AMU. . . .	C ADDR	01D5H	A	400# 4 ? 462 467
INPUT.	C ADDR	0099H	A	177 18 #
IP	D ADDR	00B8H	A	164
IS_SWAP. . . .	C ADDR	01E0H	A	395 40 #
ISO_IN	C ADDR	0232H	A	455 46 #
LAST_OUTPUT. .	C ADDR	01FEH	A	392 42 #
LAST_SWAP. . .	C ADDR	0213H	A	429 43 #
LOAD_TIMERS. .	C ADDR	015CH	A	313 31 #
NE_LAST. . . .	C ADDR	01E6H	A	403 41 #

```
N A M E          T Y P E   V A L U E      ATTRIBUTES AND REFERENCES

NOT_ECI. . . .   C ADDR    00B4H   A        188 201#
NOT_EXE. . . .   C ADDR    00C0H   A        205 207#
NOT_VR1. . . .   C ADDR    0137H   A        261 285#
NOT_VR2. . . .   C ADDR    014BH   A        285 299#
NXT_IS_LST . .   C ADDR    017BH   A        324 326 327 336#
P0 . . . . . .   D ADDR    0080H   A        [illegible]
P1 . . . . . .   D ADDR    0090H   A        [illegible]
P2 . . . . . .   D ADDR    00A0H   A        21
PAT_BIT_PTR. .   B ADDR    002FH.0 A        52# 381
PAT_DLY. . . .   B ADDR    00B0H.1 A        33# 235 240 247 380
PAT_NOT_CC . .   C ADDR    00E9H   A        234 239#
PAT_NOT_F3 . .   C ADDR    00FEH   A        239 244#
PAT_PTR. . . .   D ADDR    002EH   A        55# 141 246 332
RATIO. . . . .   C ADDR    018BH   A        307 346#
READY_LINE . .   B ADDR    00A0H.3 A        51# 169 156 196 204
RESET_INH. . .   B ADDR    00B0H.2 A        98# 179 180 191 192
RESET. . . . .   C ADDR    0000H   A        108
SET_LAST . . .   C ADDR    01F7H   A        402 404 410 420#
SET_PAT_IF . .   C ADDR    01A1H   A        358 362#
SET_RAT_CC . .   C ADDR    0195H   A        349 353#
SET_TO_ZERO. .   C ADDR    0035H   A        123# 125
SP . . . . . .   D ADDR    0081H   A        159
ST_OF_SW . . .   B ADDR    00F0H.0 A        84# 211 391 426 446
START_SWAP . .   C ADDR    022EH   A        450 458#
START_SWEEP. .   C ADDR    021DH   A        391 446#
STROBE . . . .   B ADDR    00B0H.3 A        87#
STRT_TIMER . .   C ADDR    010CH   A        236 241 249#
SV1. . . . . .   C ADDR    012FH   A        262 274#
SWEEP_EXIT . .   C ADDR    01EAH   A        412# 422 435 443
SWEEP_INT. . .   C ADDR    01C1H   A        111 390#
T1_DW_H_D. . .     NUMB    00CFH   A        32# 139
T1_DW_H_EX . .   D ADDR    003AH   A        70# 167 233 245
T1_DW_H_I. . .   D ADDR    002AH   A        68# 139 353 362 369
T1_DW_L_D. . .     NUMB    00F0H   A        33# 140
T1_DW_L_EX . .   D ADDR    003BH   A        71# 166 244
T1_DW_L_I. . .   D ADDR    002BH   A        69# 140 372
TCON . . . . .   D ADDR    0088H   A        161
TH0. . . . . .   D ADDR    008CH   A        317 412
TH1. . . . . .   D ADDR    008DH   A        167 245 373
TIMER_1_INT. .   C ADDR    01B5H   A        113 380#
TIMER0 . . . .   C ADDR    000BH   A        110
TIMER1 . . . .   C ADDR    001BH   A        112
TL0. . . . . .   D ADDR    008AH   A        318 413
TL1. . . . . .   D ADDR    008BH   A        166 244
TMOD . . . . .   D ADDR    0089H   A        162
TO_EXIT. . . .   C ADDR    01AFH   A        346 354 363 373#
TR0. . . . . .   B ADDR    0088H.4 A        212 334 340 415
TR1. . . . . .   B ADDR    0088H.6 A        214 248
VR_AMU_SWAP. .   C ADDR    0124H   A        251 265#
VR_S_D . . . .     NUMB    0004H   A        30# 137
```

```
N A M E            T Y P E   V A L U E        ATTRIBUTES AND REFERENCES

VF_S_EY. . . . .   D ADDR    0035H   A         60# 250 394 428 449
VF_S_[illegible]  . . .    D ADDR    0025H   A         59# 137
VF_SF_EDTED. .     C ADDR    0155H   A         282 297 299 312#
VF_V_[illegible] . . . . .      NUMB    0000H   A         31# 138
VF_[illegible]_FX. . . . .   D ADDR    0036H   A         62# 256 269
VF_[illegible]_[illegible] . . . . .   D ADDR    0026H   A         61# 138
VF . . . . . . .   B ADDR    00A0H.1 A         80# 258 259 266 2[illegible]7 406 407 439 440 459 460
VR . . . . . . .   B ADDR    00B0H.4 A         75# 280 290 305 3[illegible]6 307
[illegible]FC. . . . . . .   B ADDR    00B0H.5 A         76# 278 292 293 2[illegible]4 295 304 463 464 465 466
[illegible]F[illegible]. . . . . . .   B ADDR    00B0H.6 A         77# 279 291 306
WAI[illegible] . . . . . .   C ADDR    0090H   A         177# 182
WAITING. . . . .   C ADDR    0093H   A         172#
WAITINGLLR . . .   C ADDR    008EH   A         176# 197 335 341 373


REGISTER BANK(S) USED: 0


ASSEMBLY COMPLETE, NO ERRORS FOUND
```

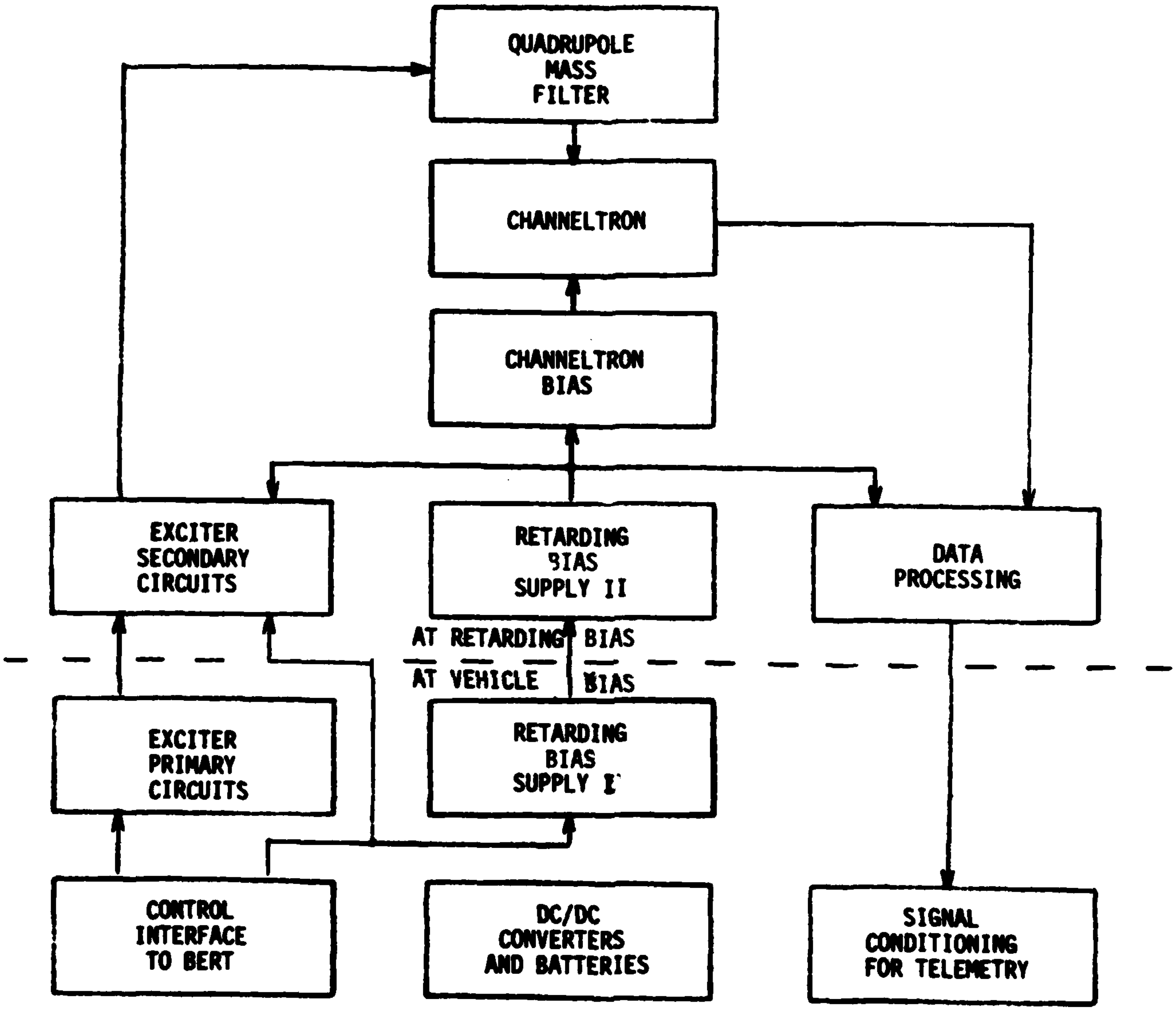


FIGURE 1. BLOCK DIAGRAM OF EIMMA

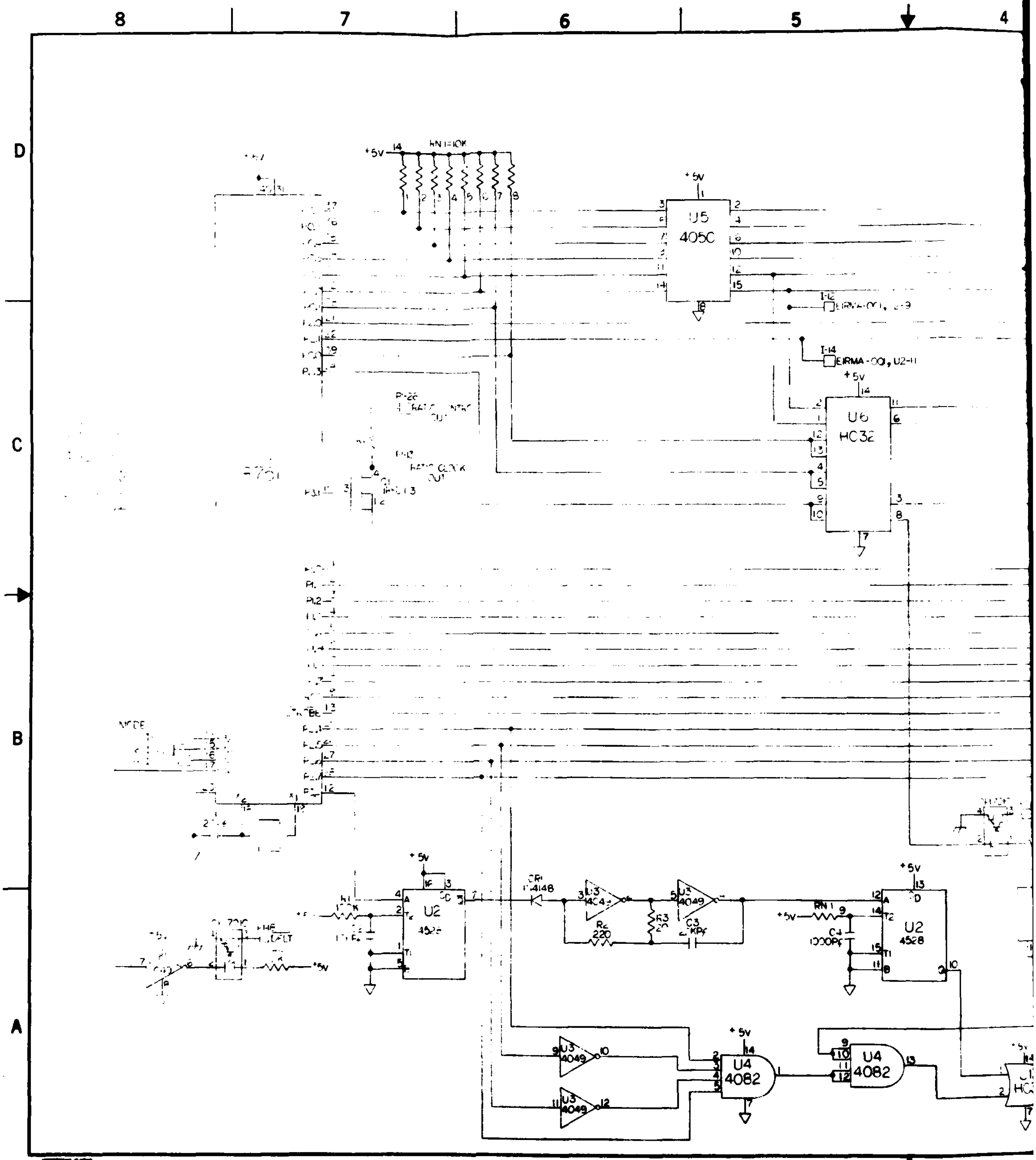
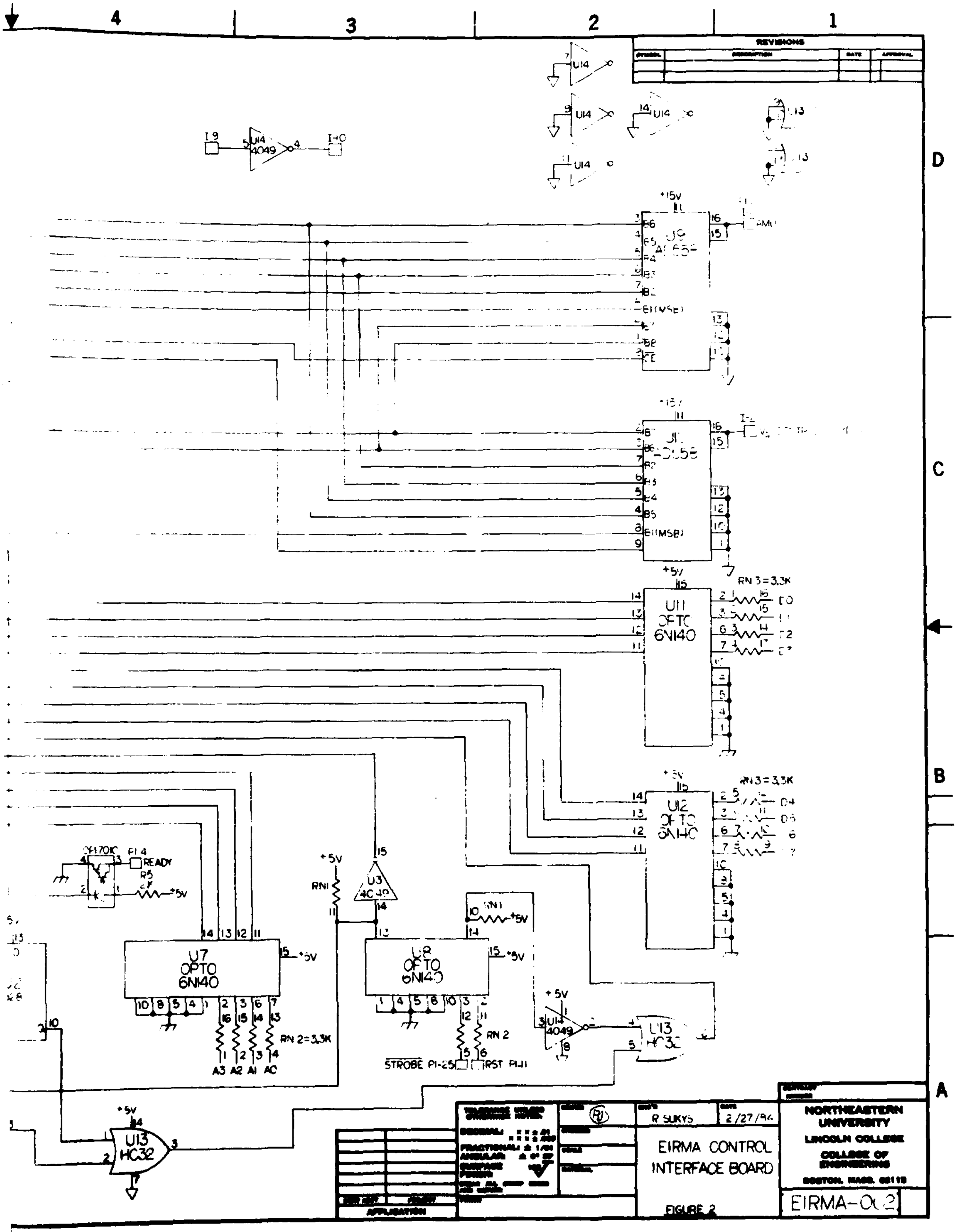


FIGURE 2. CONTROL INTERFA



2

ITROL INTERFACE

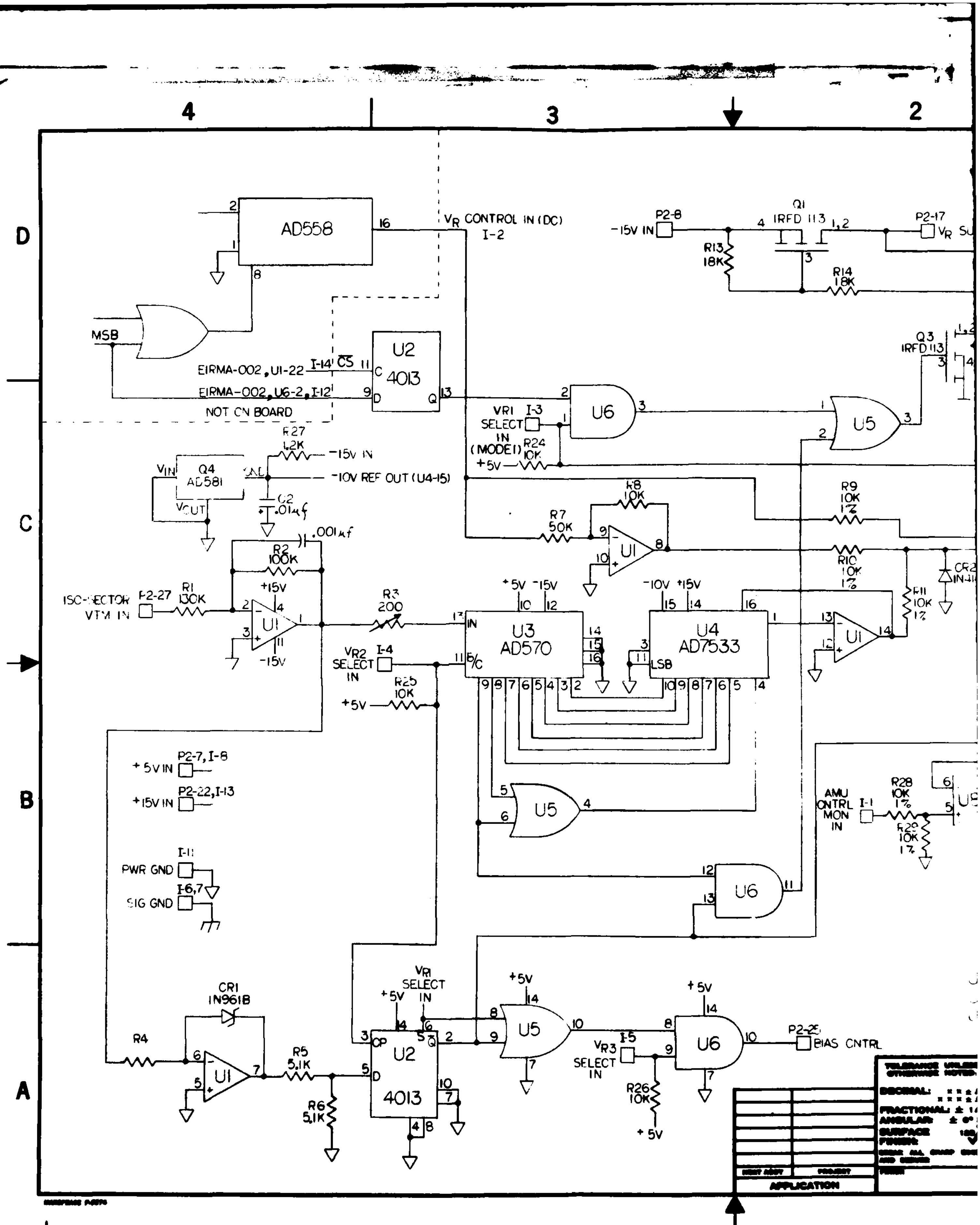
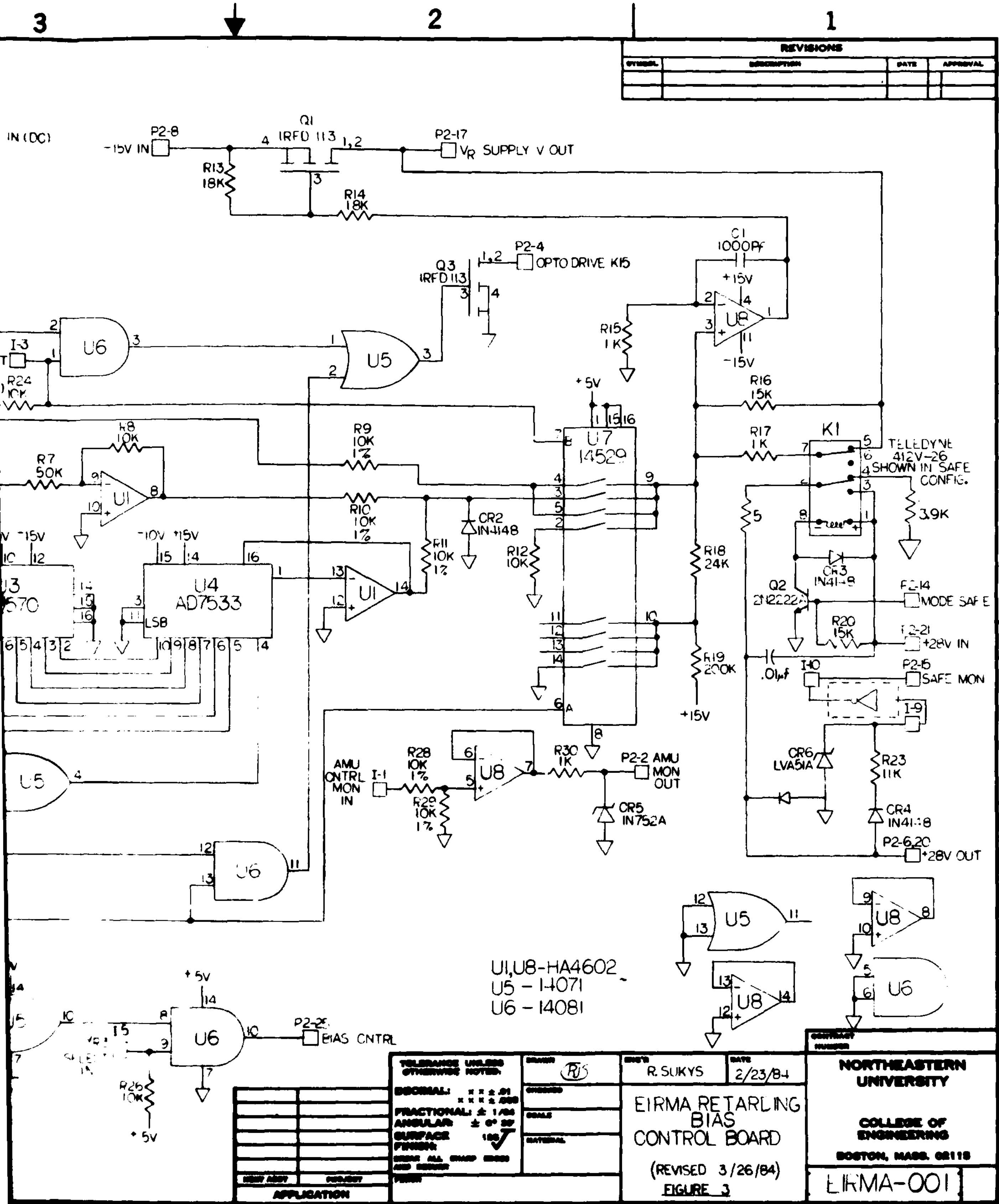


FIGURE 3. RETARDING BIAS CONTROL



2

FIGURE 3. RETARDING BIAS CONTROL

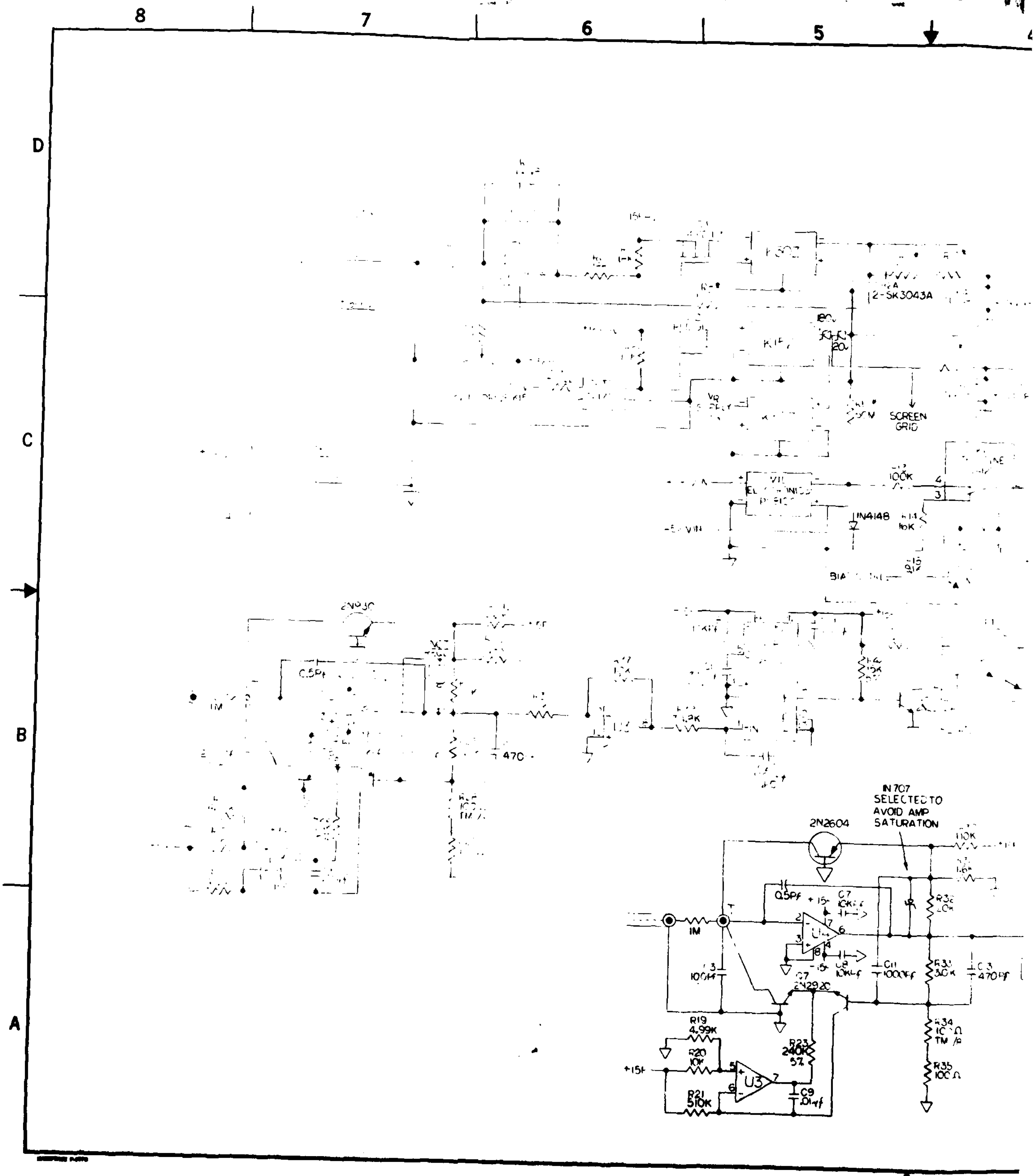
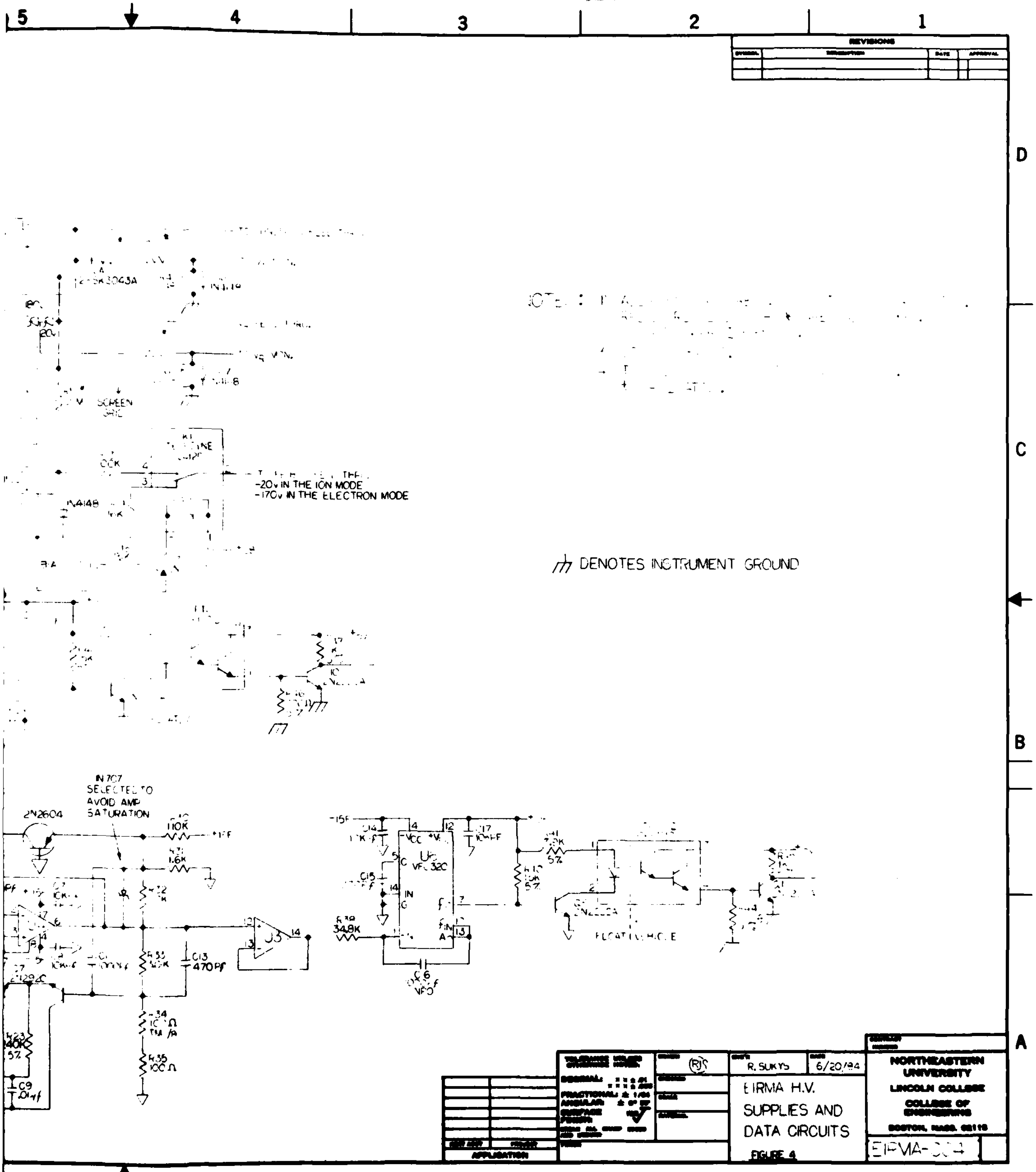


FIGURE 4. HV SUPPLIES AND DAT



2

4. HV SUPPLIES AND DATA CIRCUITS

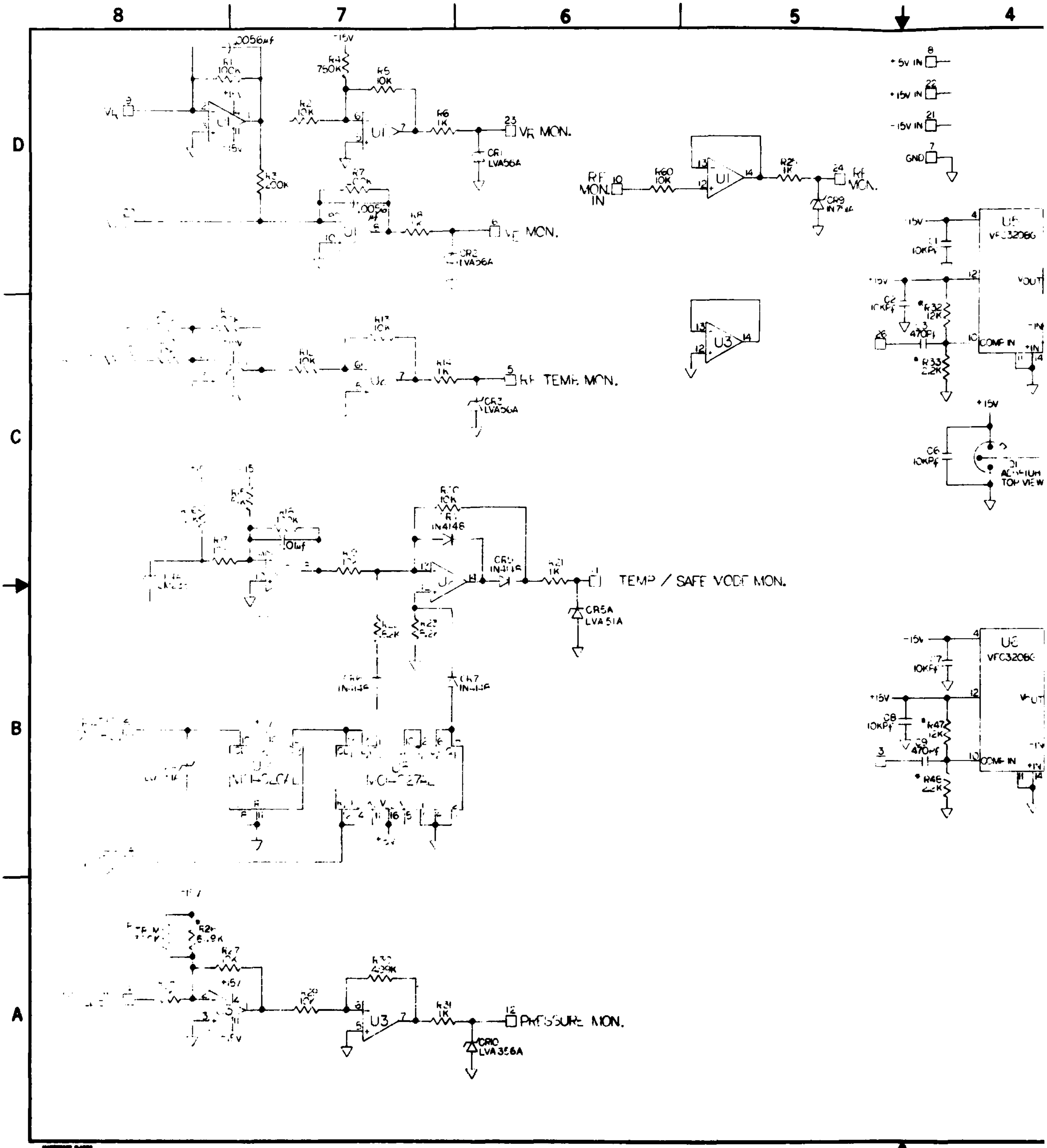
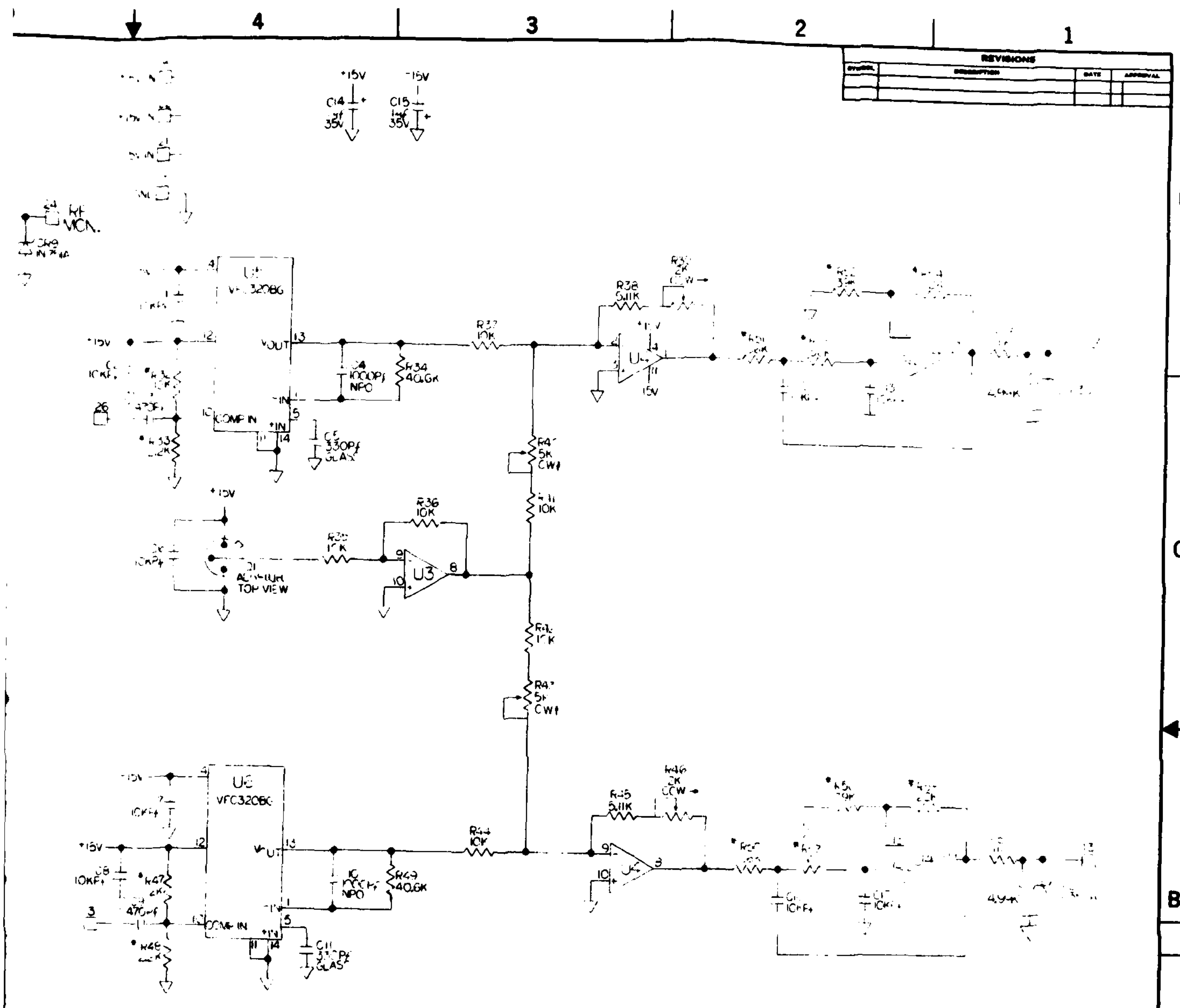


FIGURE 5. SIGNAL CONDITIONING CIR



NOTES : 1) U1–U4 ARE HARRIS 4002.
2) RESISTORS DENOTED BY * ARE 1/4 W, 5%, ALL ...

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EIRMA SPECT. FLUX SIGNAL COND. CIRCUITS & EIRMA MONITORS

FIGURE 5

EIRMA-C03

APPLICATION

2

SIGNAL CONDITIONING CIRCUITS

VI. PERSONNEL

A list of the engineers who contributed to the work reported is given below:

J. Spencer Rochefort, Professor of Electrical and Computer Engineering and Principal Investigator.

Raimundas Sukys, Senior Research Associate, Engineer.

VII. RELATED CONTRACTS AND PUBLICATIONS

F19628-74-C-0042	1 September 1973 through October 1976
F19628-76-C-0256	1 August 1976 through 31 October 1978
F19628-78-C-0218	15 September 1978 through September 1981
F19628-81-C-0162	15 September 1981 through present.

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